**CPU Design Project – Part 5 – Hardware Implementation and a Working**

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1. What did you learn from this project?

This project has helped me to understand the core parts of the basic CPU. I am getting familiar with VHDL and FPGA board, which I barely get contact in my research study. With the specific design experiences from basic components in the datapath to the top-level CPU, the process reinforced every physical concepts introduced during the lecture and gave us a better understanding. It is a fun process to learn the CPU in this way.

1. What would you do differently next time?

If I had the chance to do this project again, firstly I would like to try the pipeline datapath implementation. After several courses’ study, the pipeline datapath turns out not so complex and maybe realizable. After dealing with the clock delay issue in the multicycle I think the pipeline may be a better option to synchronize the process without conflict of the source. Secondly, I would learn about the basic FPGA hardware at the first time before I begin the implementation of the multicycle datapath. So I wouldn’t need to go back to change the origin design to make it compatible with the hardware, such as the length of the address in the memory and the display method on the FPGA board.

1. What is your advice to someone who is going to work on a similar project?

I advise the others who are going to work on this similar project to start early and prepare well with the basic knowledge of VHDL (or Verilog HDL). Getting familiar with the related software tools and experienced debug process are critical to increase the efficiency of the project design. Besides the multicycle datapath has a bunch of clock delay issue in the implementation process, it would be much easier if the datapath design had taken it into consideration at the first time.

At the beginning of the project design I wouldn’t consider the memory implementation as a big challenge. However, it turned out the produced memory is not compatible with our datapath and control unit. Since the memory unit is produced by the Quartus’ wizard tool, it is difficult to debug it as normal as other units. Eventually with right memory downloaded on the FPGA board, which is shown on the “In-system memory content editor”, there is still no result shown on the LED light. I would presume no memory data is transformed to the datapath and control unit. While running Modelsim to simulate the results in the memory unit, we ran into the problem of no results shown at all with the clock running. If we had more time to do it, I would start checking from the data transforming path between memory and datapath and control unit, since all the simulation results of the datapath and control unit performs positive in the Modelsim simulation with the forcing address value. Besides this, the memory checking with Modelsim tool is also crucial to make sure it is a working unit independently.