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**What did you learn from this project?**

This project taught me that simulation on Modelsim, doesn’t necessary to be synthesized. This is because of the real time implementation of our design. The most important thing was don’t include combinational logics in process statement. This mistake led us too many unwanted latching in our design. Then we discussed with our TA and she suggested her to check the possibility of memory elements. This practice made us re design few elements in our project.

Before starting the project we had a plan in our mind to design and synthesize the CPU. But the operational design we understood in debugging phase. According to me this project gave me great detail on synchronous and asynchronous elements and how they handshake together.

**What would you do differently next time?**

Next time, we would try to implement either single cycle data path or Pipelining Architecture. With single cycle data path we would like to implement new instructions. In pipelining taking care of data hazards would be challenging and fun. Plug and play would be fun.

**What is your advice to someone who is going to work on a similar project?**

It is better to start the project early and meet all the time lines as they are designed to complete the project in the right time. It is good to test each component in the board after simulating it. Be simple in design and analyze and test the design thoroughly during simulation because when it is implemented on the board things will seem oblivious and hard to debug. As long as you get output and results working, it’s a fun project.