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Part 5, CPU design project, ELEC 6200

**What did you learn from this project?**

CPU design project helped us in better understanding of datapath and practical difficulties and situation that we should take care deliberately in designing our digital system next time. We get close to practical implementation broaden our theoretical background.

I have learnt code debugging, designing a datapath of my own, and get much more familiar to Altera Quartus II software and FPGA board.

**What would you do differently next time?**

I would like to build analog microprocessor next time using CML logic gates. I’ll use this datapath that I designed. Main drawback will be I won’t have any specific design automation tool, but it is possible to build using scripting. BJT based micro-processor will be much faster than CMOS technology due to Gm efficiency, low-leakage and less parasitic at higher operating frequency and I hope I can shoot it up to 7-10GHz.

**What is your advice to someone who is going to work on a similar project?**

Please read the problem specification before you start. I believe memory specification was not very well. It is asynchronous, that means reading is always possible if you give any address to pc.

I used double edge trigger, for which I needed positive edge first, but in push switch it comes negative edge first. Then I flipped the clock and realize pc is incrementing but it is not reading from memory.

My memory had mem\_en and rd\_wr which means, memory is active when mem\_en is high, and then you can read or write based ond rd\_wr. But it was not true. There were no mem\_en and there was only write enable (rd\_wr=1 means write). So I left mem\_en open and flip my rd\_wr (in my case rd\_wr=1 meant read) but it did not work.

First I tried for 16 bit wide address with 8K words and then I had to change it to 16 bit wide and 256 long because FPGA board does not have that much memory. Also, for the address bus, 3 upper most bits should be left open.

Also, in answering part 4, answer 7 I followed proper direction and generated memory.v which was not successfully compiled because in Verilog, it do not support some packages from Altera. So if you import one, you’ll find it has some other dependency.

Because I performed 13 instruction verification in simulation except two memory operations, I believe my datapath was perfectly ok, but it could read memory and did not show any thing in the register file.