

Fig. 2 Equivalent resistor model of resistor stage

To provide large resistance, transistor M1, M2, M3 and M4 work at saturation region in our design. As shown in Fig.2. Equivalent ground resistances  $R_{o10}$  and  $R_{o5}$  are very large compared to  $r_{o1,2,3,4}$  and they can be neglected in the resistance calculation. Then the resistance between point A and B can be expressed as:

$$R_{AB} = (r_{o3} + r_{o4}) \parallel (r_{o1} + r_{o2}) = \frac{1}{I_{eff} (\lambda_n + \lambda_p)} \quad (2)$$

Where  $r_{o1,2,3,4}$  is the output resistance of transistors M1, M2, M3 and M4.  $\lambda_n$  and  $\lambda_p$  are channel length modulation parameters. And  $I_{eff}$  can be expressed as:

$$I_{eff} = \frac{I_A \times I_B}{I_A + I_B} \quad (3)$$

Due to symmetric design for the resistor stage,  $I_A$  and  $I_B$  are identical. Then the tunable CMOS resistor is achieved, the resistance equals to:

$$R = \frac{1}{I_{S1} \left( \frac{\lambda_n + \lambda_p}{2} \right)} \quad (4)$$

As shown in equation (4), the resistance is inversely proportional to bias current  $I_{S1}$ . It can be easily adjusted via changing transistor's bias current  $I_{S1}$  and  $I_{S2}$ . Sweeps of tunable resistor are shown in Fig.3. In Fig.3,  $V_T$  (x-axis) is the voltage adding on the tunable resistor and  $I_{out}$  (y-axis) is the current flow out from the tunable resistor. The bias current  $I_{S1}$  is shown on the top of Fig.3. The simulation result validates that the tunable resistance is inversely proportional to bias current. Fig 4 shows the resistance variation as bias current changing. Both resistance and bias current  $I_{S1}$  are in logarithm scale. As Fig.4 shown, the resistance can be tuned from 90K ohm to 40M ohm by

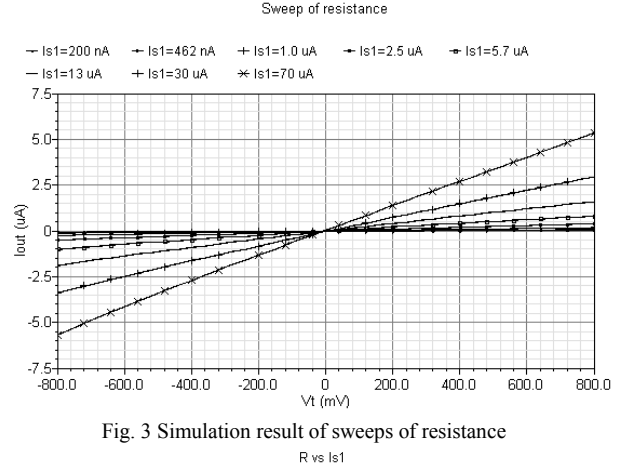


Fig. 3 Simulation result of sweeps of resistance

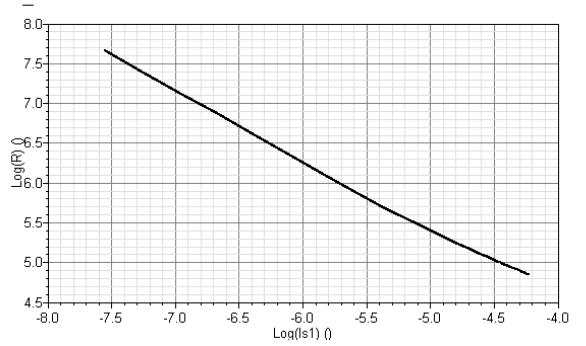
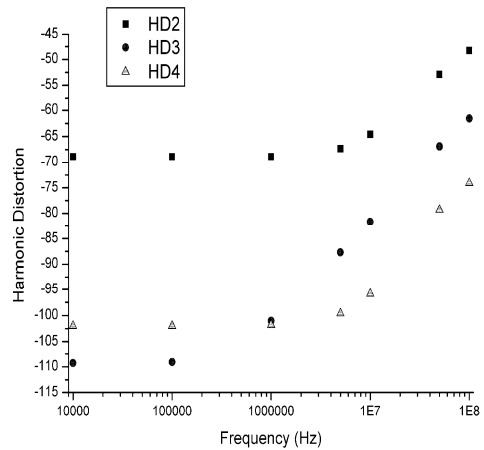


Fig. 4 Resistance variation as current changing (resistance and current are both in logarithm scale)

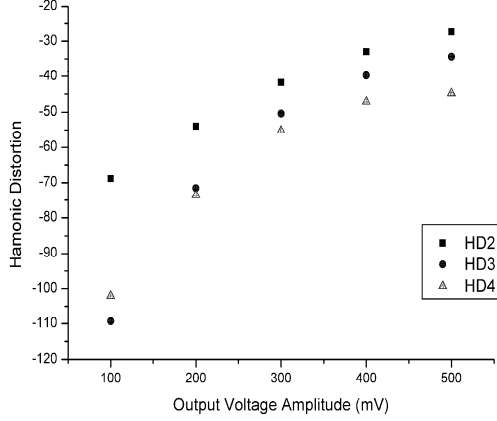
directly changing the bias current. Compared to traditional Gm cell, in which the tuning range is determined by square root of bias current, and MOSFET working in triode region to act as a resistor, the CMOS resistor in our design has much wider resistance tuning range and larger resistance.

Fig.5 shows the linearity performance of tunable resistor. Fig.5 (a) illustrates the harmonic distortion of tunable resistor under different frequency when output signal amplitude is held at 100mV. As shown, the second harmonic distortion determines the THD, which is below -48dB when frequency is lower than 50MHz. Fig.5 (b)



(a)

### III. IMPLEMENTATION OF TUNABLE FILTER IN VLSI TECHNOLOGY



(b)

Fig. 5. Experimental linearity results of tunable resistor for different frequency and different output power. (a) Harmonic distortion for different input signal frequency. (b) Harmonic distortion for different output signal amplitude

shows the harmonic distortion of tunable resistor as signal amplitude swept. The frequency of input signal is kept at 500 kHz. Both (a) and (b) show that second order harmonic distortion is the dominated nonlinearity factor. Thus, reduction of distortion can be obtained by using the tunable resistor in balanced structures.

#### B. Low Pass Filter

As mentioned above, the input impedance of the CMOS resistor is much larger than output impedance. Thus, they can be cascaded directly. A simple way to implement a second-order low-pass RC filter with proposed tunable resistor is shown in Fig.6. As shown, tunable resistors and capacitors are simply connected to compose a low-pass filter.

Since tunable resistor's pole frequency is far away from filter's pole frequency, its influence on low frequency pole can be neglected. Simple RC low-pass filter has a second order pole located at:

$$p = -\omega_c = -\frac{1}{RC} = -\frac{I_{S1} \left( \frac{\lambda_n + \lambda_p}{2} \right) I_{S1}}{C} \quad (5)$$

As shown above, the cut-off frequency can be directly tuning via changing bias current.

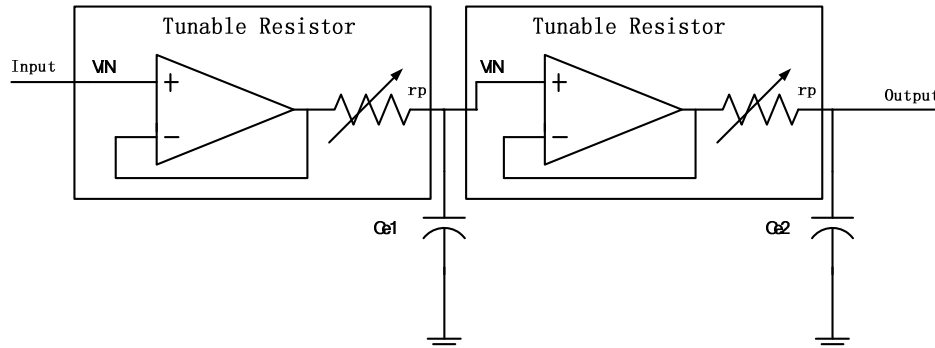


Fig.6 Simplify schematic of second-order low pass filter based on tunable resistor

As an example, a second-order tunable low pass filter using the CMOS resistor as discussed above is implemented and measured. The circuit has been fabricated in 0.5- $\mu\text{m}$  CMOS technology. The conceptual schematic of low pass filter is shown in Fig.6. The total filter block occupies  $0.25\text{mm} \times 0.13\text{mm}^2$  as shown in Fig.7. The tunable resistor block is as same as shown in Fig.1. Two tunable resistors in the filter are identical; differences will occur due to manufacturing tolerances. In case separate externally tuning is necessary.

To reduce influence of parasitic parameters and temperature, metal isolation metal (MIM) capacitor was chosen to implement capacitors Ce1 and Ce2.

#### IV. MEASURED RESULT

The filter was packaged in  $2\text{mm} \times 2\text{mm}$  QFN package. Fig.8 shows the measured amplitude response of filter when input signal level is  $300\text{mV } V_{p-p}$ . As shown, the cutoff frequency can be widely tuned from 5 kHz to 1.9 MHz as current control voltage changing from 0.75V to 0.95V. The cutoff frequency is a little bit lower than simulation result due to the influence from parasitic capacitor of package and PCB board.

The linearity performance of the low pass filter is shown in Fig.9. The input signal frequency is set at 500 kHz when cutoff frequency is at 1.5MHz. The THD of the tunablefilter is -40dB when input amplitude is  $100\text{mV } V_{p-p}$  and -34dB when input amplitude is  $200\text{mV } V_{p-p}$ .

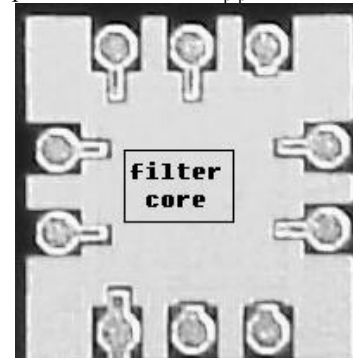


Fig. 7 Die photo of tunable low pass filter

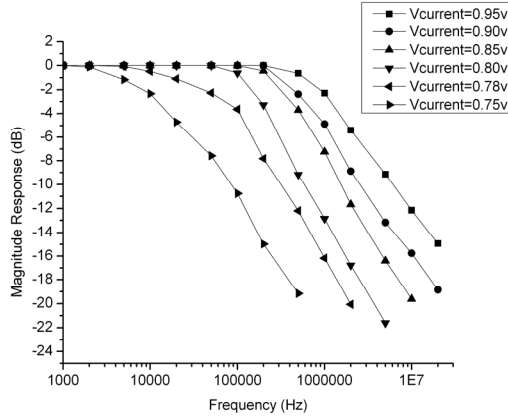


Fig.8. Measured amplitude response of tunable low pass

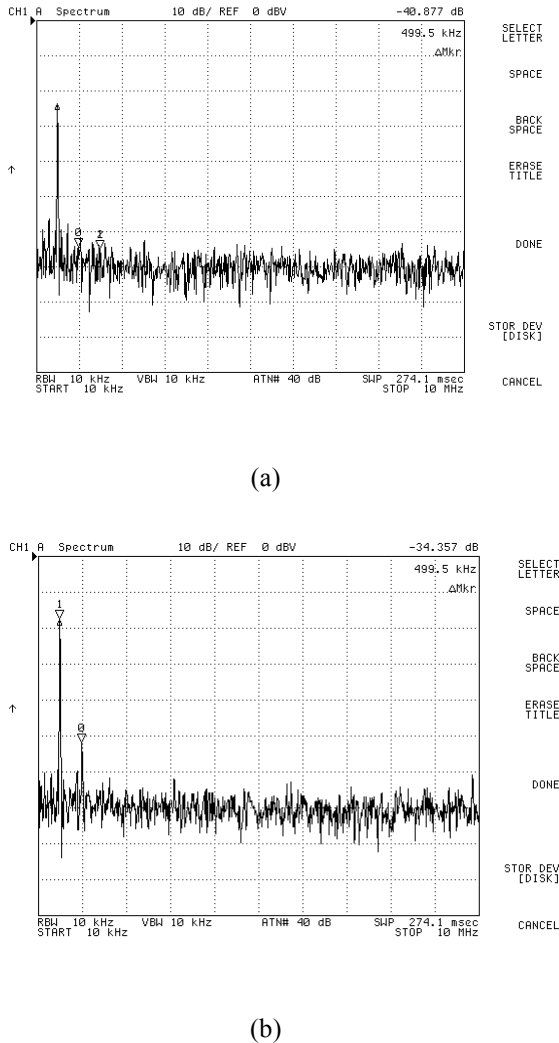


Fig.9. Measured output spectrum of the second-order low pass filter at: (a) input signal level of 100mV V<sub>p-p</sub> (b) input signal level of 200mV V<sub>p-p</sub>

A summary of the measured performance of the proposed filter is shown in Table I.

Table I. Summary of Measured Performance of the Proposed Filter

	This work	Ref [2]
Technology	0.5- $\mu$ m CMOS	0.18- $\mu$ m CMOS
Power Supply	3.3 V	1.8V
Cutoff frequency range	5k - 1.9M Hz	0.5M - 12MHz
Frequency tuning range Freq <sub>max</sub> /Freq <sub>min</sub>	380	24
Power Consumption (maximum cutoff frequency)	5.7mW	4.7mW
Power Consumption (minimum cutoff frequency)	2.8mW	1.1mW
f <sub>-3dB</sub> variation for V <sub>cc</sub> 3.1V-3.8V	$\pm 3.4\%$	--
Core Size	0.0325 mm <sup>2</sup>	0.125 mm <sup>2</sup>

## V. CONCLUSION

In this paper, a new CMOS tunable resistor has been designed and analyzed. Its main characteristics are: wide resistance tuning range, large resistance, low power consumption, and small die size. The resistance can be tuned by directly changing bias current. The performance of the proposed tunable resistor has been demonstrated by realizing a second-order low-pass RC filter in 0.5- $\mu$ m CMOS technology. The measured result shows that the cutoff frequency can be tuned from 5 kHz to 1.9 MHz. The THD is -40dB at an input signal level of 100mV V<sub>p-p</sub>. Although no automatic tuning was addressed in this paper, it is emphasized that automatic tuning schemes for the CMOS resistor we discussed are unavoidable.

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