
About the Cover

The integrated circuit consists of approximately 100,000 transistors and was designed by the author in 1981-1982. This was the first chip at Bell Labs to incorporate Built-In Self-Test (BIST) and the first BIST approach for embedded Random Access Memories (RAMs). The BIST circuitry is included in the lower portion of the chip (as indicated in the floor plan below) and is used to test the 8K-bit RAM. A refined version of this BIST approach was integrated in the automatic generator for RAMs in 1986. The RAM generator with BIST was then used to create the RAMs for all standard cell Application Specific Integrated Circuits (ASICs) designed at Bell Labs.

