

ELEC 5970/6970 BIST

Assignment #8 Scan-Based BIST (Graduate Students Only)

Implement a hierarchical scan-based BIST for your circuit according to the following specifications:

1. CUT: Implement full scan (all flip-flops) with a single scan chain and without input isolation multiplexers (you can connect your PIs directly to the TPG for this implementation).
2. TPG: Implement an LFSR-based TPG with primitive polynomial of size to satisfy the design guidelines to minimize linear dependencies for $N_{TV} = 255$.
3. ORA: Implement a MISR of size $\max\{N_{PO}+1, 16\}$ to compact all primary outputs plus your scan chain output.
4. CONTROL: Implement a BIST controller with Shift and Pattern Control for proper initialization and control of BIST sequence as well as output response compaction. Your design should include an active high BIST Start input and active high BIST Done output. Note: you can only assume one clock cycle of BIST Start being inactive for initialization purposes (in other words, you cannot assume that it will be inactive for multiple clock cycles for initialization purposes – your BIST controller will be responsible for complete initialization).
5. The top level design should have the following input and output ordering. Note that your TPG, ORA, and BIST controller should be separate subcircuits from your s# CUT although your s# CUT will include the scan flip-flops. Also note that you must not use the “scan vector” capabilities of AUSIM, all initialization, controllability, and observability must come from the BIST circuitry in conjunction with the PIs and POs given below for the top level circuit.
 - a. Input ordering: CLK, BISTStart (no other inputs)
 - b. Output ordering: BISTDone, MISRoutputs (no other outputs)

Record (or calculate) the following data for your fault simulation with collapsed faults for the complete circuit with BIST and for each of the four subcircuits (CUT, TPG, ORA, and BIST controller):

Total number of faults:

Number of faults detected:

Number of potentially detected faults:

Fault coverage:

In addition, report the following information:

Number of clock cycles until BIST Done goes active:

$P(x)$ for your TPG LFSR:

Area overhead in terms of number of gates:

Area overhead in terms of gate I/O:

Plot cumulative fault coverage as function of vector count for the complete circuit.

Describe your BIST controller design including the number of clock cycles used for Shift count and Pattern count.

Show that the degree of $P(x)$ meets the design guidelines for linear dependencies.

Email your complete an final ASL to me prior to the beginning of class on the day the assignment is due so that I can simulate and verify your results. Turn the remainder of the material in on paper at the beginning of class on the day the assignment is due. Note that this assignment counts at least 20% of your total homework grade.

For the last time (we hope) – Happy BISTing!!!!