

## ELEC 5280/6280 BIST

### Assignment #7 Circular BIST

Read the “Instructions for Circular BIST Tools” (included in new AUSIM.zip file) on the AUSIM web page to get an overview of the CAD tools for Circular BIST that are included in the AUSIM.zip file. Note that you have already used `cbistext.exe` in earlier assignments. You will also need to copy the `cbist.lib` file (also included in new AUSIM.zip) to your working directory. Then you will need to do the following steps:

1. Extract your flip-flops using `cbistext` and put your list of flip-flops in a file called `s#e.scn`.
2. Generate 1000 clock cycles of a Circular BIST sequence using `cbistvec` with 0 reseeds. Note that 1000 CBIST vectors is 1000 clock cycles with both vectors for the full clock cycle and the program also provides several clock cycles of initialization sequence in the vector set using the Circular BIST control signals B0 & B1. Also note that there is a “scan scanc” AUSIM command at the end of the vector set and a file called `scanc` was created with 0s for each flip-flop; this will have the effect of “scanning” out the final CBIST signature at the end of the fault simulation.
3. Insert the Circular BIST flip-flops and input isolation multiplexers using `cbistinr` (note that you should use 0 for the `muxff` parameter since we will only be using input isolation multiplexers for this assignment).
4. Run a parallel fault simulation for collapsed single stuck-at gate level faults. Note that you need to include “lib `cbist.lib`” in your AUSIM control file. Also include a `flipro` command in your control file.
5. Remove the faults associated with the CBIST circuitry using `cbistrmf` and rerun the fault simulation using the modified fault list as the input fault list to AUSIM. This will give the effective fault coverage obtained for the system function in the original circuit.
6. Re-order your flip-flops in the Circular BIST chain using `cbistran` with 2 for the `seed_value`, re-insert the CBIST flip-flops and isolation MUXs using `cbistinr` for the new ordering, and rerun the fault simulation. Note that reordering the Circular BIST chain is one hardware solution to register adjacency.

Record (or calculate) the following data for each of your three parallel fault simulations (two orderings of the CBIST chain and one simulation without the CBIST circuitry faults included):

Total number of faults:

Number of faults detected:

Number of potentially detected faults:

Fault coverage (assuming potential detect probability = 0.5):

Did all primary outputs initialize?

Calculate the CBIST area overhead in terms of #G and #Gio using the method from the last assignment (Gates w/DFT vs Gates w/o DFT – from audit file).

Use the results from the fault profile to plot the per vector cumulative fault coverage as a function of the vector count for the two orderings of flip-flops in the Circular BIST chain and the simulation with CBIST circuitry faults removed. Include all three profiles on the same graph to compare the variation with respect to flip-flop ordering and consideration of effective fault coverage.

Turn in your results on paper at the beginning of class on or before the assigned deadline.