

ELEC 5280/6280 BIST

Assignment #5 Pseudo-Random Test Pattern Generators

For each of the three TPGs listed below:

1. Draw a logic diagram labeling all inputs and outputs for a rising edge triggered implementation with active high synchronous preset (to the all 1s state).
2. Write an ASL description for the TPG with input ordering: CLK PRESET.
3. Generate a set of vectors (with no clock-data races) that will first initialize and then take the TPG through its *complete* sequence (note that the same set of vectors should work for all TPG designs).
4. Run a logic simulation to verify the maximal length sequence and debug as needed.
5. Run a fault simulation and modify your vector set as needed to obtain 100% fault coverage (assume probability of potential detect = 1). Note that for each LFSR there are at least 10 faults that can only be potentially detected).

Note: Any XOR gates in your designs (both logic diagram and ASL) can only have two inputs.

The three TPGs are:

- A. Internal feedback LFSR of degree 5
- B. External feedback LFSR of degree 5 *with* the ability to generate the all 0s pattern.
- C. A 5-bit cellular automata register with null boundary conditions and Rule 90 and 150 combinations of XXOOX where the X can be your choice of Rule 90 or Rule 150 while the O represents the other rule.

For each TPG, turn in on paper at the beginning of class on or before the specified deadline:

- Complete logic diagram
- ASL description (.asl file)
- Simulation results (.out file)
- Fault coverage

Happy TPGing!!