

ELEC 5970/6970 BIST

Assignment #4 Test Pattern Generators

Design the following three TPGs:

1. A maximal length internal feedback LFSR of degree 5
2. A maximal length external feedback LFSR of degree 5 with the ability to generate the all 0s pattern.
3. A 5-bit cellular automata register with null boundary conditions and Rule 90 and 150 combinations of XXOOX where the X can be either Rule 90 or Rule 150 while the O represents the other rule.

For each of the three TPGs:

- A. Draw a logic diagram for a rising edge triggered implementation with active high synchronous preset (to the all 1s state).
- B. Write an ASL description for the TPG with input ordering: CLK, PRESET.
- C. Generate a set of vectors (with no clock-data races) that will first initialize and then take the TPG through its complete sequence (note that the same set of vectors should work for all three TPG designs).
- D. Run a logic simulation to verify the maximal length sequence and debug as needed.
- E. Run a collapsed gate-level stuck-at fault simulation and modify your vector set as needed to obtain 100% fault coverage. Assume the probability of potential detect = 1, and note that for the LFSRs there are 10 faults that can only be potentially detected (all others can be detected).

For each TPG, turn in on paper:

- Complete logic diagram
- ASL description (.asl file)
- Simulation results (.out file)
- Fault coverage with list of undetected and potentially detected faults

For each TPG, email me your:

- ASL description (.asl file)
- Input vector file (.vec file)

Happy TPGing!!