ELEC 5970/6970 BIST

Assignment #3 Random Scan Test Patterns

Generate 200 random test patterns for scan design testing of your circuit using the random vector generator but this time you will use some additional options to generate scan vectors. Note that there are no scan flip-flops in your circuit but AUSIM can simulate your circuit as if scan design were implemented (but without the shifting in of the test vectors so the simulation should be fairly fast). Use the following parameter and options:

ranvec *s#.vec* 200 *#ins* scan *#ffs*

where s# is the name of your assigned circuit, *#ins* is the number of primary inputs to your circuit (not counting the clock input), and #*ffs* is the number of DFFs in your circuit. You can get the *#ffs* number by first generating the scan chain file for your circuit by typing:

cbistext *s#.asl s#.scn*

The *s#.scn* file generated by this command will be needed by AUSIM for your scan chain flip-flop ordering during the simulation. For now, we will assume the default ordering produced by the *cbistext* program is sufficient. Note that the *ranvec* program will generate 201 files (*s#.vec* plus 200 scan input vector files, *scan0-scan199*). During logic simulation a scan output vector file will be generated for each scan input vector file, labeled *scan0o-scan199o*, which give the output results from the scan out operation.

Make sure you vector set *s#.vec* to matches your ASL name *s#.asl*. Run a parallel fault simulation for both collapsed and uncollapsed single stuck-at gate level faults and record the time required for each simulation. Run a serial fault simulation for dominant bridging faults.

A. For you circuit and logic simulation record the following:
1. The number of DFFs in your circuit
2. Did all primary outputs initialize (look at simulation results in s#.out)?
3. Calculate the area overhead for the implementation of full scan in your circuit in terms of:
   a) #G - assuming 3 gates/MUX and 9 gates/FF (note that DFFs are only counted as 1 gate in AUSIM)
   b) #G_{IO} - assuming 9 G_{IO}/MUX and 25 G_{IO}/FF (note that DFFs are only counted as 4 G_{IO} in AUSIM)

   Be sure to show your calculation work (how your are calculating area overhead).

B. Record the following data for each of your three fault simulations:
1. Total number of faults:
2. Number of faults detected:
3. Number of undetected faults:
4. Number of potentially detected faults:
5. Fault simulation time:
6. Fault coverage (assuming x=1 for potentially detected faults):

C. Use the results from the fault profile to plot the individual fault coverage and cumulative fault coverage as a function of the vector count for collapsed and uncollapsed gate level parallel fault simulations.

Turn in your results on paper at the beginning of class on or before the specified deadline.

Note: after completing all of your simulations you will want to delete the scan# files since there will be 400 of them. They can easily be reproduced by re-executing *ranvec* followed by a logic simulation.

Happy BISTing!!