

ELEC 5970/6970 BIST

Use the ASL for the circuit assigned to you (get the ASL for circuit assigned to you from the class web page); this circuit will be used for all of your assignments. Also you will need to download the AUSIM.zip file for the PC executable workstation version of AUSIM and other tools from the class web page and extract the files.

Assignment #1 Random Test Patterns

Generate 2000 random test patterns for your circuit using the random vector generator (ranvec.exe) included in the AUSIM.zip file. To execute this program, type the following:

```
ranvec s#.vec 2000 #ins
```

where *s#* is the name of your assigned circuit and *#ins* is the number of primary inputs to your circuit (not counting the clock input). You will need to look at the ASL description to get the number of inputs.

Make sure your vector filename prefix (*s#.vec*) matches your ASL filename prefix (*s#.asl*) and make a dummy library file (an empty file or a file with just a comment) named *s#.lib*. Run a serial and a parallel fault simulation in for both collapsed and uncollapsed single stuck-at gate level faults and record the time required for each simulation. The following control files give examples for logic and fault simulations (note that the logic simulation only needs to be ran one time with the simulation results in *s#.out* used for subsequent fault simulations):

For serial collapsed faults with audit:

default <i>s#</i>	
proc	
audit	(generates audit file)
simul8	(logic simulation)
fltgen	(generates fault list)
fltsim	(serial fault simulation)

For parallel uncollapsed faults w/o audit but with fault profile:

default <i>s#</i>	
proc	(processes ASL description)
uncol	(generates uncollapsed fault list)
fltgen	
pftsim	(parallel fault simulation)
fltpro	(fault profiling)

Record the following data for your circuit (this information will be in *s#.aud*):

- Total number of primary inputs (not counting the clock input) outputs
- Total number of primary outputs
- Total number of gates
- Total number of gate I/O
- The three primary inputs with the highest number of loads (give input name and number of loads)

Record (or calculate) the following data for your simulations:

1. Logic Simulation: Record the logic simulation time (given at end of logic simulation). Did all primary outputs initialize? Did they stay initialized? (look at simulation results in *s#.out*).
2. Fault Generation: Total number of collapsed and uncollapsed faults (these faults will be in *s#.flt*):
3. Fault Simulation: Number of faults detected (these faults will be in *s#.det*), undetected (these faults will be in *s#.udt*), and potentially detected (these faults will be in *s#.pdt*) for both collapsed and uncollapsed faults:
4. Fault Simulation: Record fault simulation time for parallel and serial fault simulation for both collapsed and uncollapsed faults (given at end of fault simulation).
5. Fault Coverage: Calculate fault coverage considering potentially detected faults with 0.5 and 1.0 probabilities for collapsed and uncollapsed faults.
6. Fault Coverage: Plot individual and cumulative fault coverage as a function of the test vector number (fault detection profile information is in *s#.pro*) for collapsed and uncollapsed faults (either from serial or parallel fault simulation).

Turn in your results on paper at the beginning of class on or before the due date (be sure to include your *s#* next to your name on the sheet(s) of paper).

Happy BISTing!!!