

## ELEC 5280/6280 BIST

### Assignment #1 - Random Test Pattern Logic Simulation

Use the ASL for the circuit assigned to you (get the ASL for circuit assigned to you from the class web page); this circuit will be used for all of your assignments. Be sure to save the ASL file as *s#.asl* (where # is the circuit number assigned to you) and not as *s#.txt* or *s#.asl.txt*. Also you will need to download the AUSIM.zip file for the PC executable workstation version of AUSIM and other tools from the class web page and extract the files. To download the AUSIM.zip, click on “AUSIM software, manuals, and notes” link on the class web page, then click on the “download workstation version of AUSIM that runs on Windows” link. Read the AUSIM manual.

Generate 2000 random test patterns for your circuit using the random vector generator (*ranvec.exe*) included in the AUSIM.zip file. To execute this program, type the following in a DOS command prompt window in the directory containing the *ranvec.exe* executable:

```
ranvec s#.vec 2000 #ins
```

where *s#* is the name of your assigned circuit and *#ins* is the number of primary inputs to your circuit (not counting the clock input). You will need to open and look at the inputs “ckt:” statement in ASL description of your circuit to count the number of inputs or use the number given in the comment lines at the top of the ASL file.

Make sure your vector filename prefix (*s#.vec*) matches your ASL filename prefix (*s#.asl*) and make a dummy library file (an empty file or a file with just a comment) named *s#.lib*, where # is the number of your circuit. The following control file give example for logic and fault generation:

For logic simulation with audit file and collapsed stuck-at-fault generation:

```
default s#  
proc  
audit  
simul8  
fltgen
```

Run a logic simulation using the control file above by typing in the directory where *ausim.exe*, your ASL file, vector file, and control file are located:

```
ausim s#.test
```

where *s#.test* is the name of your control file.

A. Record the following data for your circuit from the audit file (*s#.aud*):

1. Total number of primary inputs (not counting the clock input)
2. Total number of primary outputs
3. Total number of gates
4. Total number of gate I/O
5. Total number of D flip-flops
6. Total number of fan-out stems
7. Total number of nets
8. Number of uncollapsed gate-level stuck-at faults
9. Number of collapsed gate-level stuck-at faults
10. The three primary inputs with the highest number of loads (give input name and number of loads)

B. Record (or calculate) the following data from your simulation:

1. Logic Simulation: Record the logic simulation time (given at end of logic simulation). Did all primary outputs initialize? Did they stay initialized? (look at simulation results in *s#.out*).
2. Fault Generation: number of collapsed (these faults will be in *s#.flt*). Does this agree with the audit file?
3. Fault Generation: number of uncollapsed faults (re-run AUSIM but first add “uncol” before the fltgen command in the control file). Does this agree with the audit file?

Turn in your results on paper at the beginning of class on or before the due date (be sure to include your *s#* next to your name on the sheet(s) of paper). Happy BISTing!!!