

ELEC 5970/6970 Special Topics: Built-In Self-Test

Section 001 Fall 2008 (MWF 1:00-1:50pm BR306)

Dr. Charles E. Stroud Office: 325 Broun Hall Office hours: 12-1pm and 2-3pm MWF

Textbook (recommended): *A Designer's Guide to Built-In Self-Test*, Charles E. Stroud., Springer, 2002.

Goals: This course introduces the student to the design and implementation of Built-In Self-Test techniques for digital and mixed-signal circuits. The student is also introduced to digital system testing through fault modeling, fault simulation, and design for testability.

Course Objectives:

1. An understanding of the testing process and its impact on design and manufacturing.
2. An understanding of fault modeling, detection, and simulation techniques.
3. The ability to generate test patterns to detect faults and fault models in a digital circuit.
4. The ability to implement Built-In Self-Test techniques.
5. Hands-on experience with Computer-Aided Design (CAD) tools for fault simulation.

Prerequisites by topic:

1. Digital logic design and analysis or switching theory
2. Electronics and MOS transistors

Course Outline:

Week	Lecture Topics	Chapter
1	Overview of BIST, Manufacturing and System Test	1
2	Fault Models and Detection	2
3	Fault Simulation	2
4	Design for Testability	3
5	Test Pattern Generation	4
6	Test Pattern Generation, Test #1 9/26	4
7	Output Response Analysis	5
8	Manufacturing and System-Level Use of BIST	6
9	Non-Intrusive BIST	11
10	Built-In Logic Block Observer	7
11	Circular BIST, Test #2 10/31	9
12	Scan-Based BIST	10
13	BIST for Regular Structures	12
14	BIST for FPGAs and CPLDs	13
15	Mixed-Signal BIST, Test #3 12/5	14
16	Semester review – Final Exam Wed. 12/10 12-2:30pm	

Method of evaluating student performance: There will be three exams (contributing 20% each to the course grade) and a comprehensive final exam (contributing 20% to the course grade) in addition to homework/design projects (contributing 20% to the course grade). All exams will be closed-book, closed-notes, and closed-neighbor. There will be no unannounced quizzes. All projects and assignments must be turned in on or before the designated date/time to receive credit.

Class attendance and behavior: Students are expected to attend class regularly and on time. In case of absence, the student is responsible for all course business conducted in class. There should be no distractive talking or cell phone usage during class.

Computer usage: Fault modeling and simulation assignments will require the use of the digital logic circuit simulation program AUSIM. Access to and information regarding this CAD tool is available on the class web page www.eng.auburn.edu/~strouce.