

Overview of BIST - Organization

- Overview of Testing
 - ❖ Why test?
 - ❖ What do we test for?
- Product Life Cycle
 - ❖ Manufacturing Test
 - ❖ System Operation and Test
- The Testing Problem
- What is BIST? How Does It Work?
 - ❖ Basic BIST Architecture
 - ❖ A Simple BIST Design
- Advantages & Disadvantages of BIST

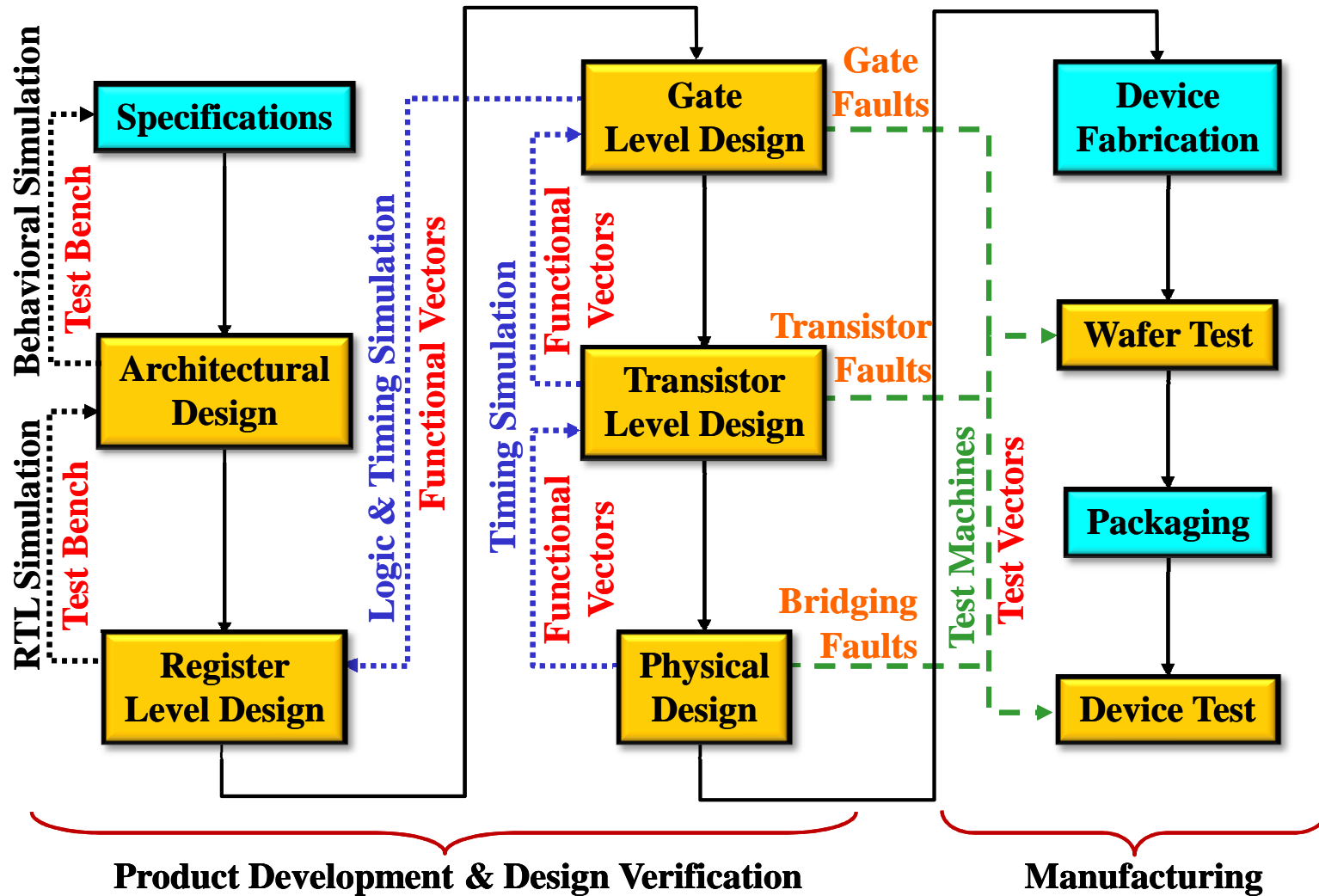
Overview of Testing

- Purpose of testing is to detect:
 - ❖ **Design errors** during development process
 - Design verification via logic & timing simulation
 - ❖ **Defects** sustained during the manufacturing process
 - Evaluation of test effectiveness via fault simulation
 - Application of tests via test machines at:
 - Wafer level
 - Device level
 - Board level
 - System level (sometimes system acts as test machine)
 - ❖ **Faults** occurring during system operation
 - On-line testing with Error Detection/Correction Codes
 - Off-line testing with system-level diagnostic tests
- “A fault causes an error which causes a system failure”

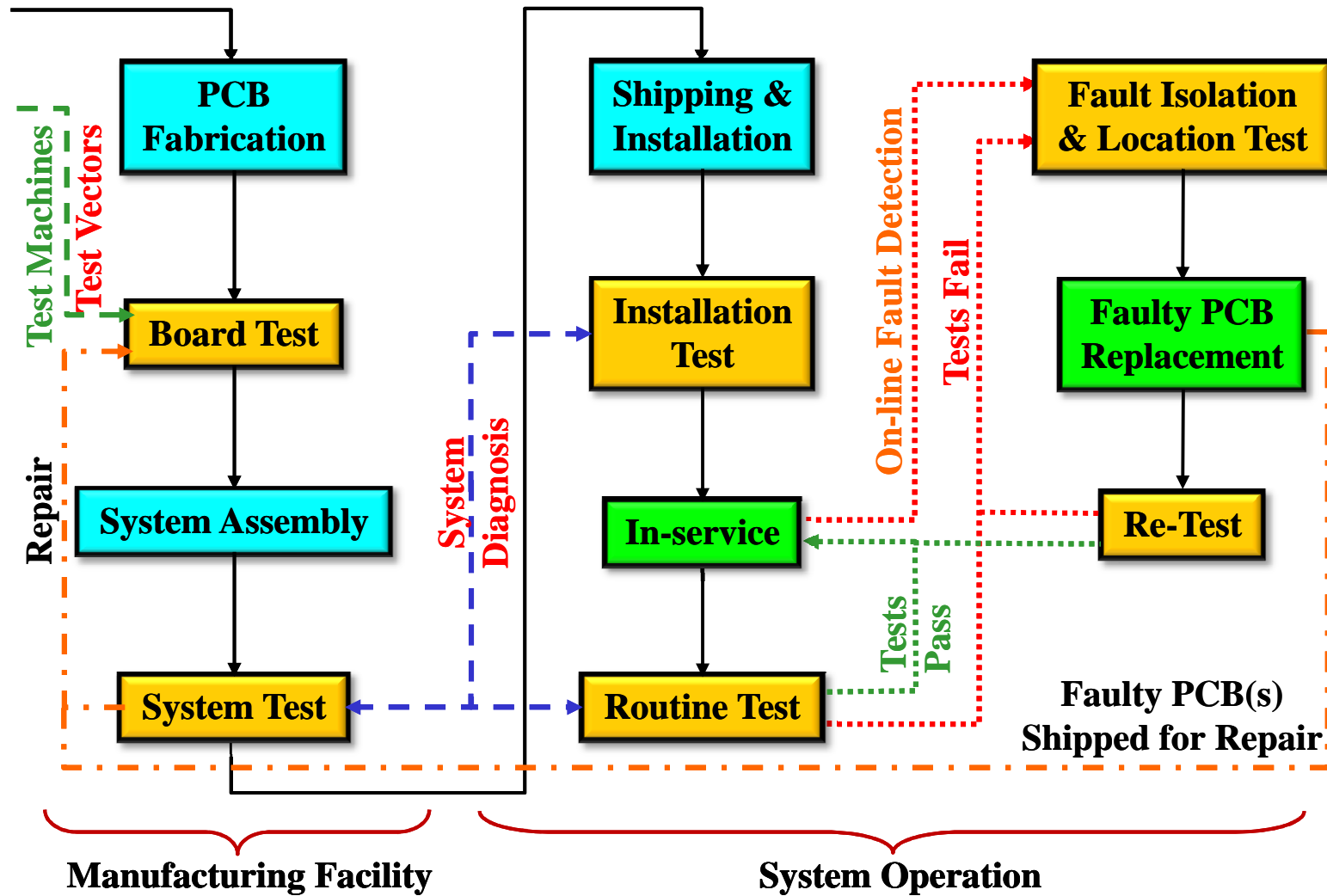
Overview of Testing (cont.)

- Testing during the product life cycle depends on:
 - ❖ Application
 - Toy or home appliance – manufacturing testing only
 - Nuclear missile launch system – testing throughout life cycle
 - ❖ System reliability & availability
 - Downtime requirements
 - Cost resulting from downtime
 - ❖ System complexity
 - Repair requirements & repair costs
 - ❖ Cost of product returns
 - Customers' perception of product quality
 - ❖ Product liability costs
- Designers/Test Engineers must consider product life cycle

Typical Product Life Cycle



Continued Life Cycle for Complex Systems



Comments on Product Life Cycle

- Simple, inexpensive, consumer products
 - ❖ Relative simple system level testing
 - ❖ May throw away faulty PCBs
 - Too expensive to repair
- Complex, expensive, highly reliable/available products
 - ❖ Require complex system-level testing
 - To ensure fault-free working system
 - To identify faulty replaceable components
 - ❖ Will have faulty PCBs repaired
 - PCBs in excess of \$1K
 - Too expensive to throw away
- Most systems fall somewhere between these two extremes

The Testing Problem

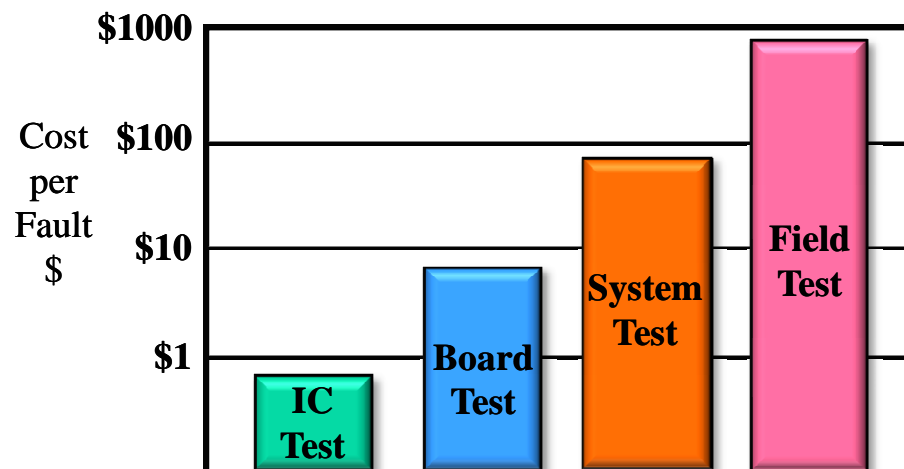
- Circuit complexity is increasing
 - ❖ More than 100 million transistors/chip is common
 - Largest chips currently over 1 billion
 - ❖ Embedded cores \Rightarrow chips \Rightarrow boards \Rightarrow systems
 - ❖ Mixed-signal chips and systems (digital & analog)
 - ❖ New technologies introduce new types of faults
- Risk of manufacturing/fabrication defects is increasing
 - ❖ Larger die size: more area \Rightarrow more defects
 - ❖ Smaller feature size: thinner & closer lines \Rightarrow more opens/shorts
 - ❖ New defect models: closer lines \Rightarrow more cross-talk
 - ❖ Higher performance: more critical paths \Rightarrow more delay faults

The Testing Problem (cont.)

- Test accessibility is decreasing
 - ❖ ICs have more gates & fewer pins
 - Pin count increased 3 orders of magnitude in 40 years
 - Transistor count increased 8 orders of magnitude in 40 years
 - ❖ 2-sided surface-mount components & multi-layer PCBs
 - In-circuit testing is no longer feasible
- Cost of developing tests is increasing
 - ❖ **Dataquest**: 22% of development cost (1988) \Rightarrow 40% (1998)
 - Manual test development requires 12 to 24 people-months
 - ❖ Algorithmic complexity of test CAD tools ($N = \#$ gates)
 - Logic simulation = $O(N)$, fault simulation = $O(N^2)$, ATPG = $O(N^3)$
 - “Classical” fault models are no longer accurate
 - ❑ Accurate fault models are difficult to simulate/emulate

The Testing Problem (cont.)

- Automatic Test Equipment (ATE) cost is increasing
 - ❖ Production ATE to test a \$50 VLSI chip > \$1M
 - *Sematech* predicts chip tester in 2010 will cost ~ \$20M
 - Most people agree we are already there
 - It costs more to test a transistor than to manufacturer it
 - ❖ At-speed testing needs more expensive ATE
 - Product testing goes on long after design is complete
 - ❖ Cumulative testing cost must be considered
 - ❖ Cost of fault location/identification and repair

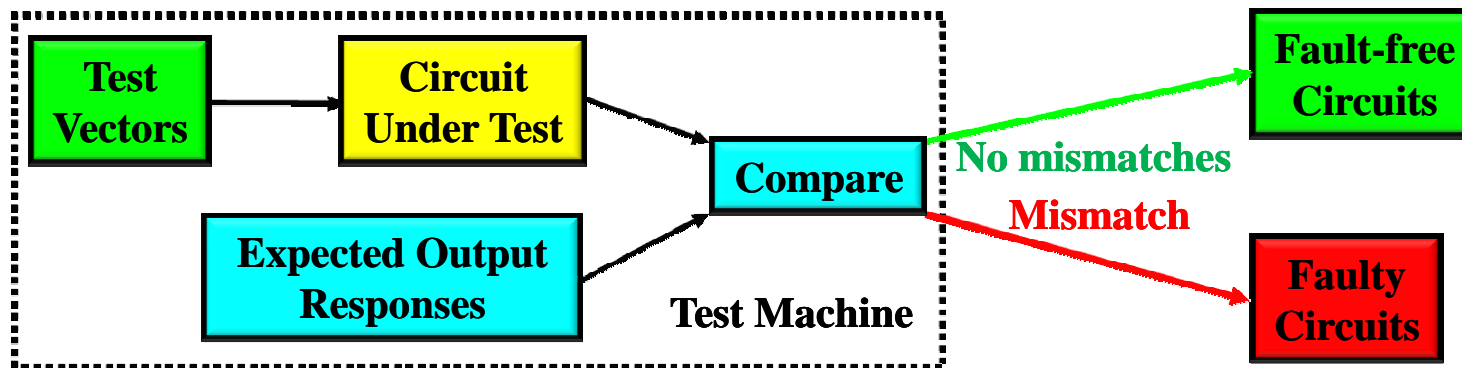


Note:

Sun Microsystems
claims multiplier > 10
for complex systems

Basic Test Process

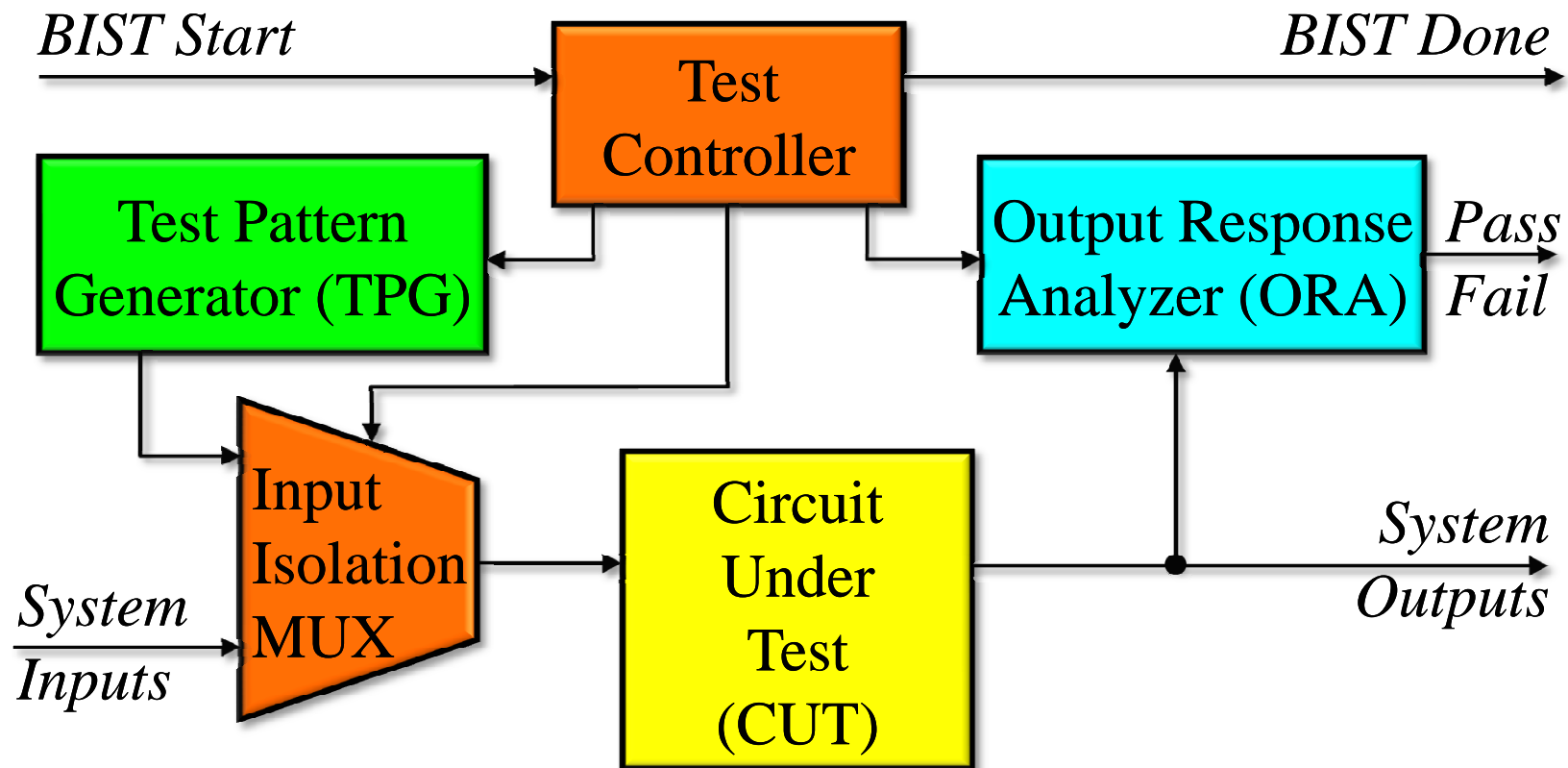
- Test Machine:
 - ❖ Applies input test patterns (aka test vectors) to CUT
 - ❖ Compares CUT output response to known good circuit output response
 - For the given set of input test patterns
 - Usually obtained from simulation
- CUT gives correct response to all test vectors
 - ❖ Assumed to be fault-free
- CUT gives incorrect response to 1 or more text vectors
 - ❖ Assumed to be faulty



What is BIST? How does it work?

- *“... the ability of logic to verify a failure-free status automatically, without the need for externally applied test stimuli (other than power and the clock), and without the need for the logic to be part of a running system.”* - [Richard Sedmak, ITC'80](#)
- *“... any of the methods of testing an integrated circuit (IC) that uses special circuits designed into the IC. This circuitry performs test functions on the IC, and signals whether the parts of the IC covered by the BIST circuits are working properly.”* - [SEMATECH Official Dictionary Rev 5.0](#)
- *“The basic idea of BIST, in its most simple form, is to design a circuit so that the circuit can test itself and determine whether it is ‘good’ or ‘bad’...”* - [C. Stroud, A Designer's Guide to BIST](#)

Basic BIST Architecture



Advantages & Disadvantages of BIST

Advantages:

- Vertical testability
 - ❖ Wafer to system
- High diagnostic resolution
- At-speed testing
- Reduced need for external test equipment
- Reduced test development time & effort
- More economical burn-in testing
- Reduced manufacture test time & cost
- Reduced time-to-market

Disadvantages:

- Area overhead
- Performance penalties
- Additional design time & effort
- Additional risk to project
- Lack of orthogonal testing