MIXED-SIGNAL BUILT-IN SELF-TEST

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Revision 3b

1. OVERVIEW OF MIXED-SIGNAL BIST

The basic mixed-signal Built-In Self-Test (BIST) architecture is shown in Figure 1 where the digital BIST circuitry that has been added to the mixed-signal circuitry is shown in bold black and the analog circuitry under test is shown in shades of grey. The normal mixed-signal system components include the digital system functions as well as the analog system functions along with the digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) that are required to convert the digital signals to analog waveforms and vice versa. The BIST circuitry includes the digital test pattern generator (TPG) and output response analyzer (ORA) functions as well as a digital test controller and analog loopback functions. The analog loopbacks (analog multiplexers) are the only circuits associated with the BIST approach to be inserted in the analog domain and, as a result, this minimizes the impact of the BIST circuitry on the operation and performance of the analog circuitry. The purpose of the analog loopback is to facilitate a return path for the test signals from the TPG, through the analog circuitry under test, and back to the ORA. An additional multiplexer (MUX) is normally required for the insertion of the digital test patterns into, and isolation of unknown system data from, the input data stream to the DAC. Since the target circuitry under test is the analog system circuits, including the DACs and ADCs, we incorporate the digital TPG and its associated MUX immediately prior to the digital inputs of the DAC. Similarly, we incorporate the digital ORA at the output of the ADC.

In order to make the BIST circuitry usable during system-level operation for off-line testing and system diagnostics, the BIST circuitry must be capable of proper initialization of the analog circuitry under test, isolation of system data inputs, and reproducible results from one execution of the BIST sequence to the next in the same manner as is required in digital systems. The length of the initialization sequence must be sufficient to clear the effects of previous system signals in the analog circuitry. Faults can be effectively isolated to a given section of analog circuitry within the diagnostic resolution of the analog loopbacks multiplexers. For example, with the left-hand analog loopback in Figure 1 activated, any faults detected are isolated to that path from the TPG to the ORA (indicated by the dark grey bordered analog circuitry and paths in Figure 1). If the BIST sequence indicates a good circuit, then the left-hand analog loopback can be deactivated while the right-hand loopback function can be activated and the BIST re-executed. Faults detected during this second BIST sequence would be isolated to the analog circuitry shown in light grey in Figure 1. Therefore, the selection of the sites for the analog loopback functions can be based on the desired diagnostic resolution and fault detection capability of the BIST approach versus the area and performance impact on the analog circuitry.

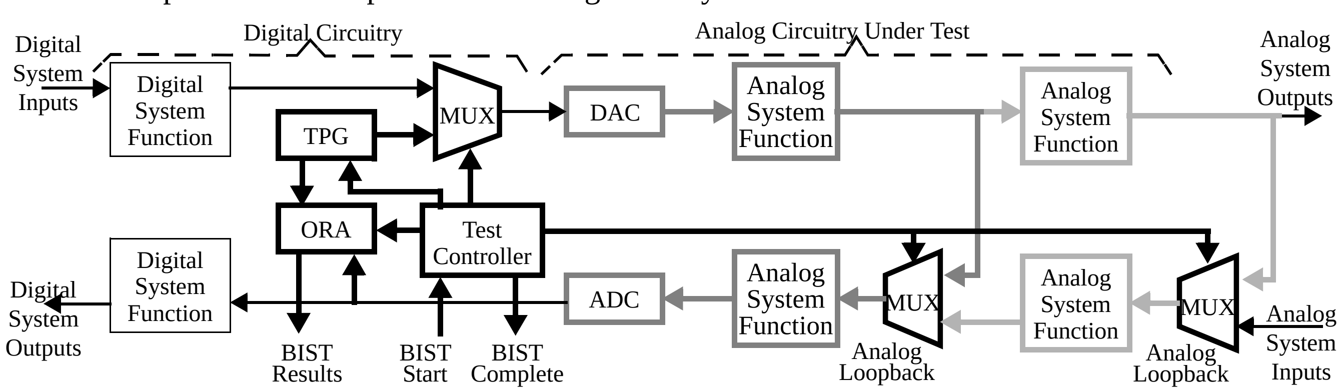


Figure 1. BIST Architecture for Mixed Signal Systems

2. Test Pattern Generator (TPG)

The TPG, illustrated in Figure 2, is an 8-bit design and includes a binary up/down counter that also functions as an external feedback Linear Feedback Shift Register (LFSR) with primitive characteristic polynomial, $P(x)=x^8+x^6+x^5+x+1$. The counter provides a variety of analog test waveforms. For example, a single pass through the up-count range produces a ramp signal at the output of the DAC while multiple passes produces a saw-tooth analog test signal. Combining a series of up/down-counts generates triangular waveforms at the output of the DAC. When in a TPG count mode (count-up, count-down, count-up/down), the increment value for the counter is supplied by the Magnitude Register and, as a result, is programmable. The LSFR mode of operation in the TPG produces an analog signal that is more noise-like. The bit reversal multiplexer reverses the order of bits to the DAC (MSBs becomes LSBs and vice versa) and has the effect of producing high frequency components in the counter modes. The TPG can produce DC, step and pulse (the width of the first complete BIST clock cycle) waveforms where the magnitude to the DAC is determined by the value into Magnitude Register. Finally, the TPG can produce a sequence of square waves with pseudo-random pulse widths by allowing the last bit in the LFSR to control the binary value to the DAC; when the last bit of the LFSR is a logic 1, the DAC gets the value specified by the Magnitude Register and when the last bit of the LFSR is a logic 0 the DAC gets an all 0s value. During a carry-out of the counter or all 1s of the LFSR, the TPG produces an active high output (TCO) to the test controller. When in a DC, pulse, or step TPG mode, the increment value for the counter is 1 such that TCO is produced every 256 clock cycles. The test waveforms produced by the TPG are summarized in Table 1.

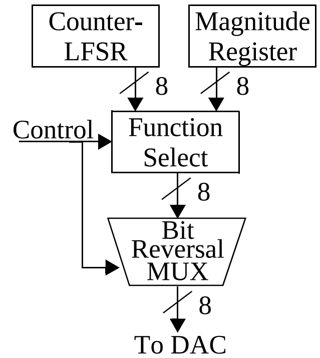
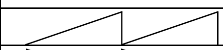
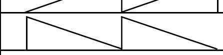
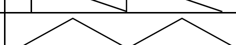
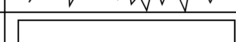
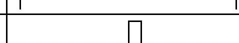
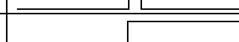
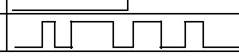


Figure 2. TPG Block Diagram

TABLE 1. Summary of test waveform produced by TPG

Digit pattern	Analog Waveform	Pictorial
count-up	saw-tooth	
count-down	saw-tooth	
count-up/down	triangular wave	
LFSR	noise	
constant magnitude	DC	
pulse	pulse	
step	step	
pseudo-random square waves	pseudo-random square waves	

3. Output Response Analyzer (ORA)

The ORA, illustrated in Figure 3, consists of a double-precision accumulator used to sum the magnitudes of the sampled output responses from the ADC. The accumulator-based ORA facilitates the determination of the pass/fail status of the BIST by expecting the final sum to be within a predetermined range of values to account for acceptable variations in the analog component parameters, voltage, and temperature as well as quantization noise in the DAC and ADC. Determination of the range of resultant values which indicates that the circuit is fault-free is based on specifications of the analog circuit responses to the various input signals produced by the TPG. In order to test the digital portion of the BIST circuitry, we loopback of the TPG output directly to the ORA input to test the digital BIST circuitry by summing the magnitudes of the test waveforms produced by the TPG and look for an exact BIST result. Therefore, the ORA sup-

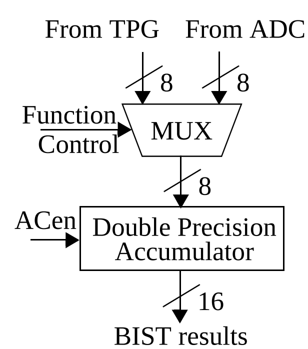


Figure 3. ORA Block Diagram

ports two separate test functions. During each test function, the various test waveforms are produced by the TPG and the resultant ORA value is read to determine the pass/fail status of each waveform. If any of the test waveforms within each of the four test function fails to produce a correct accumulator value when summing the TPG output, the BIST circuitry is considered to be faulty. When testing the analog circuit by summing the magnitudes of the analog output response to the waveforms produced by the TPG, a resultant ORA value outside the acceptable range of values for that waveform would indicate the analog circuitry under test is faulty. The accumulator can be initialized by writing data into the high (ACHI) and low (ACLO) bytes while the BIST results can be obtained by reading these bytes.

4. TEST CONTROLLER (TC)

The Test Controller, illustrated in Figure 4, consists of a 2-bit binary BIST sequence counter (BCNT) and a 1-bit status register (DONE), which are writable and readable from the Processor Interface. Note that write operations take precedence over all other operations and are synchronous. The BIST sequence is initiated by the BIST Start input (active high). When a BIST sequence is not active the BCNT counter and DONE register hold their data. The BIST Counter (BCNT) value is the number of cycles of the TPG counter/LFSR to be applied during the BIST sequence. Note that the ORA is only compacting response data during the active BIST sequence. Therefore, once the BIST control bit is activated, the number of active TPG counter/LFSR carry-out (TCO) signals is counted to achieve the number loaded into BCNT and the DONE signal is activated (active high) indicating that the BIST sequence is complete. In other words, when a BIST sequence has been initiated the following events take place:

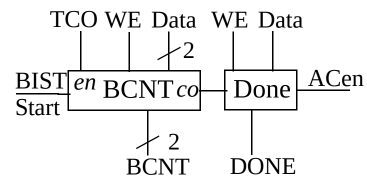


Figure 4. Test Controller Block Diagram

1. The value loaded into BCNT represents the number of TPG cycles for the BIST sequence such that when the BIST sequence is initiated, BCNT decrements on the rising edge of CLK whenever TCO=1 (except when TCO=1 corresponds to the start of the BIST sequence), otherwise it holds its value. When BCNT has counted down to all 0s, it produces a carry-out.
2. The active carry-out signal from BCNT sets DONE=1 (indicating the BIST sequence is done) on the next rising edge of CLK, otherwise DONE holds its value.
3. ACen is active (high) only when a BIST sequence has been initiated and DONE=0 which enables output response compaction in the accumulator circuit. When DONE=1, the accumulation is disabled and the ORA holds its BIST results values for retrieval via the Processor Interface.

5. PROCESSOR INTERFACE (PCI)

The Processor Interface, illustrated in Figure 5, consists of a read multiplexer and a write-enable address decoder. The read multiplexer selects data based on the two input address bits (see Register Descriptions for bit ordering and address specifications). The four write enables (WE[0-3]) are generated (active high) based on the two address bits Add1-0 and the read-write bit (RW=1), otherwise all write-enables are inactive (logic 0).

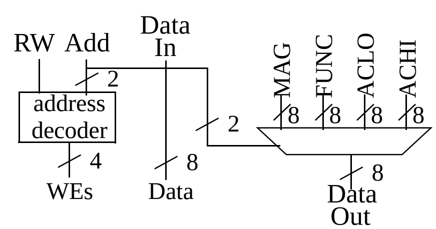


Figure 5. Processor Interface Block Diagram

6. REGISTER DESCRIPTIONS

Table 2 provides a description of the register address and bit operation descriptions for the four registers accessible via the Processor Interface. While the Magnitude Register simply supplies the Magnitude during constant amplitude test pattern sequences (including the DC test and the constant amplitude frequency sweep), the Control Register determines the TPG operation.

TABLE 2. Register Bits and Addresses

Register	Address Add 1-0	Bits							
		Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
Magnitude	00	Mag 7	Mag 6	Mag 5	Mag 4	Mag 3	Mag 2	Mag 1	Mag 0
Function	01	DONE	BCNT 1	BCNT 0	Bit Rev	TFS 2	TFS 1	TFS 0	OFS
Accum Low	10	AC 7	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0
Accum High	11	AC 15	AC 14	AC 13	AC 12	AC 11	AC 10	AC 9	AC 8

The ORA Function Select bit (OFS) determines whether the output of the TPG (OFS=0) or the ADC (OFS=1) is summed in the accumulator during the BIST sequencce. The three TPG Function Select bits (TFS 2-0) control the test patterns to be generated by the TPG (see Table 3). The Bit Reversal control bit activates the reversal of the order of bits to the DAC (and ORA) when Bit Rev = 1, otherwise the order of the bits are not reversed. Finally, the BIST Start (active high) activates the TPG test pattern sequence. When BIST Start = 0, the TPG circuit is initialized to the value specified in Table 3.

TABLE 3. TPG Function Select Bits

TFS 2	TFS 1	TFS 0	Test Pattern Generator function description	Initial Value
0	0	0	Linear Feedback Shift Register	all 1s
0	0	1	Count-up (saw-tooth) - increment value from Magnitude Reg	all 0s
0	1	0	Count-down (saw-tooth) - decrement value from Magnitude Reg	all 1s
0	1	1	Count-up/down (triangular wave) - increment/decrement value from Magnitude Reg	all 0s
1	0	0	Pseudo-random duration square waves - magnitude from Magnitude Reg	all 1s
1	0	1	DC - magnitude from Magnitude Reg	Mag Reg
1	1	0	Step - magnitude from Magnitude Reg	all 0s
1	1	1	Pulse - magnitude from Magnitude Reg	all 0s

7. INPUT/OUTPUT PIN DESCRIPTIONS

The input/output pins of the BIST circuit and naming convention and ordering to be used in this project are summarized in Table 4. The entity name for this project is MSBIST.

TABLE 4. I/O Pin Names, Ordering, and Descriptions

Inputs	No. Pins	Functional Description	Outputs	No. Pins	Functional Description
CLK	1	System clock (rising edge-triggered)	PDO7-0	8	Processor interface Data Out
BIST	1	BIST Start control	DONE	1	BIST Done
RW	1	Processor interface read/write	TPG7-0	8	TPG Data outputs (to DAC)
ADD1-0	2	Processor interface address			
PDI7-0	8	Processor interface Data In			
ADC7-0	8	Analog Data inputs (from ADC)			Total I/O pin count = 38