Overview of Testing - Organization

- Purpose of Testing
  - ⇨ Why test?
  - ⇨ What do we test for?
- Testing During the Product Life Cycle
  - ⇨ Typical Product Life Cycle
  - ⇨ Life Cycle for Complex Systems
- The Testing Problem
  - ⇨ Testing Complexity
  - ⇨ Testing Cost
- Other Testing Issues
  - ⇨ Types of Testing
  - ⇨ Testing Terminology

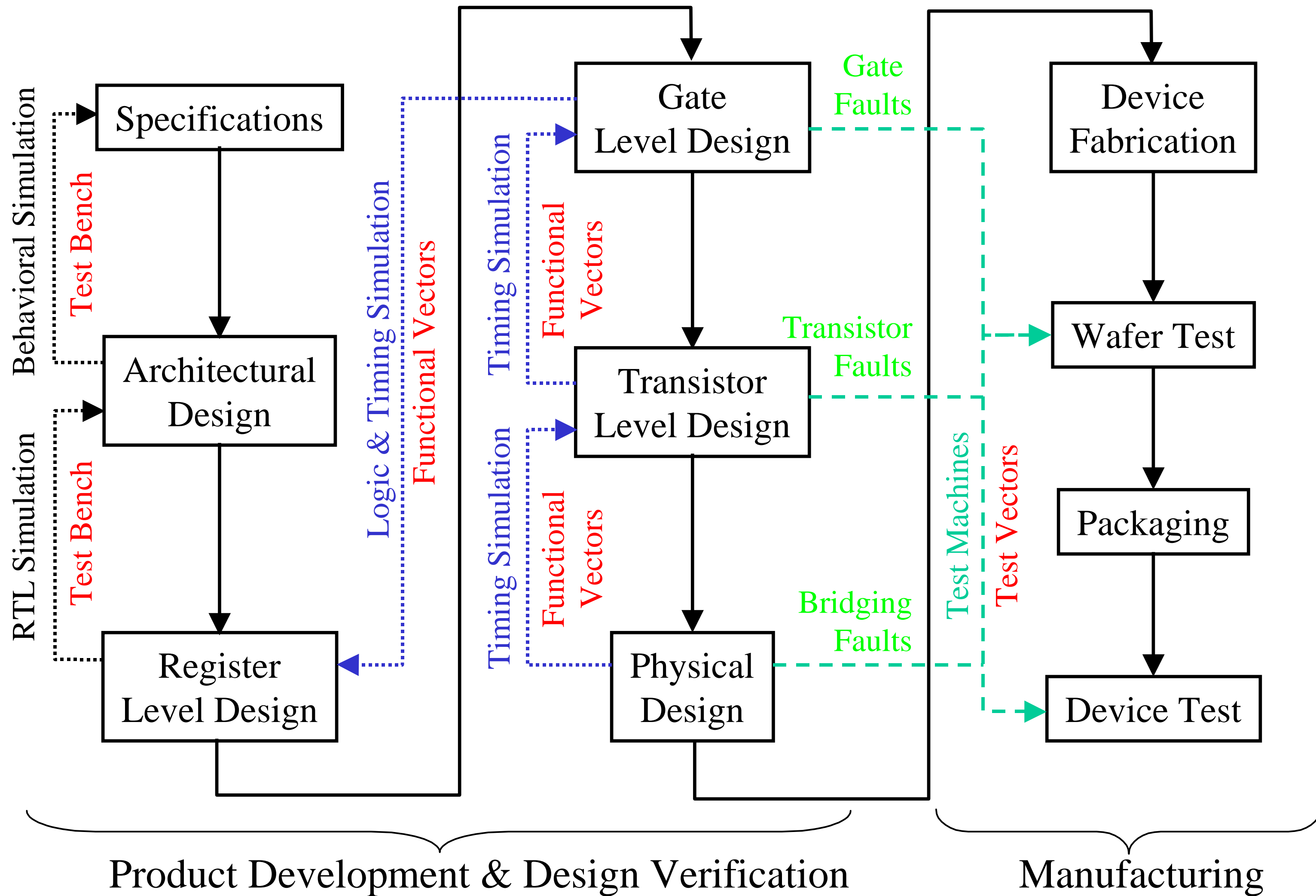
Overview of Testing

- Purpose of testing is to detect:
  - ⇨ ***Design errors*** during development process
    - ⊙ Design verification via logic & timing simulation
  - ⇨ ***Defects*** during the manufacturing process
    - ⊙ Evaluation of test effectiveness via fault simulation
    - ⊙ Application of tests via test machines at:
      - Wafer level
      - Device level
      - Board level
      - System level (sometimes system acts as test machine)
  - ⇨ ***Faults*** occurring during system operation
    - ⊙ On-line testing with Error Detection/Correction Codes
    - ⊙ Off-line testing with system level diagnostic tests

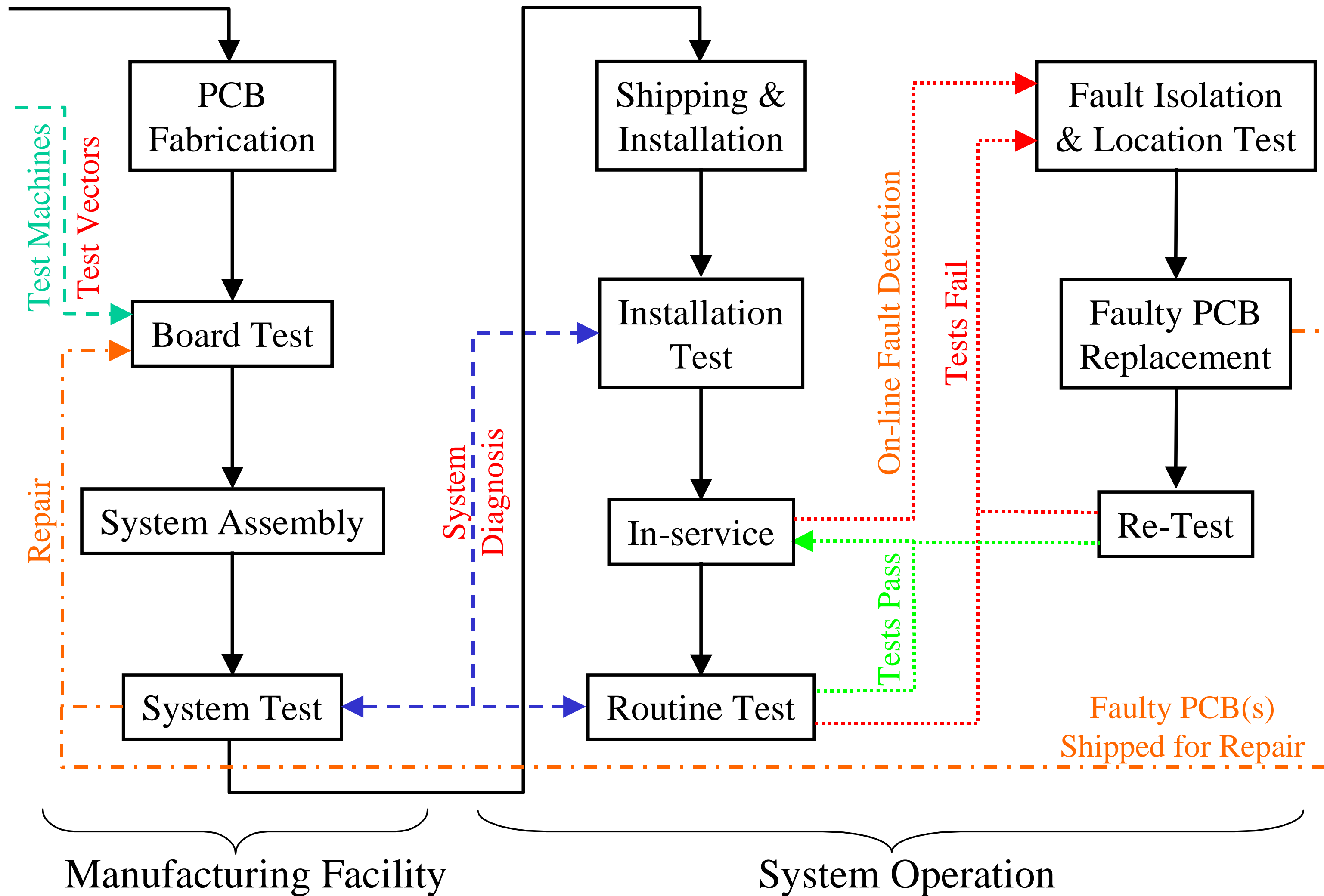
Overview of Testing (cont.)

- Testing during the product life cycle depends on:
  - ⇨ Application
    - ⦿ toy or home appliance – only manufacturing testing
    - ⦿ nuclear missile launch system – testing throughout life cycle
  - ⇨ System reliability & availability
    - ⦿ downtime requirements & cost resulting from downtime
  - ⇨ System complexity
    - ⦿ repair requirements & repair costs
  - ⇨ Cost of product returns
    - ⦿ customers' perception of quality & supplier
  - ⇨ Product liability costs
- Designers/Test Engineers must consider product life cycle

Typical Product Life Cycle



Continued Life Cycle for Complex Systems



Comments on Product Life Cycle

- Simple, inexpensive, consumer products
  - ⇨ Relative simple system level testing
  - ⇨ May throw away faulty PCBs
    - ⦿ Too expensive to repair
- Complex, expensive, highly reliable/available products
  - ⇨ Require complex system level testing
    - ⦿ To ensure fault-free working system
    - ⦿ To identify faulty replaceable components
  - ⇨ Will have faulty PCBs repaired
    - ⦿ PCBs in excess of $1K
    - ⦿ Too expensive to throw away
- Most systems fall somewhere between these two extremes

The Testing Problem

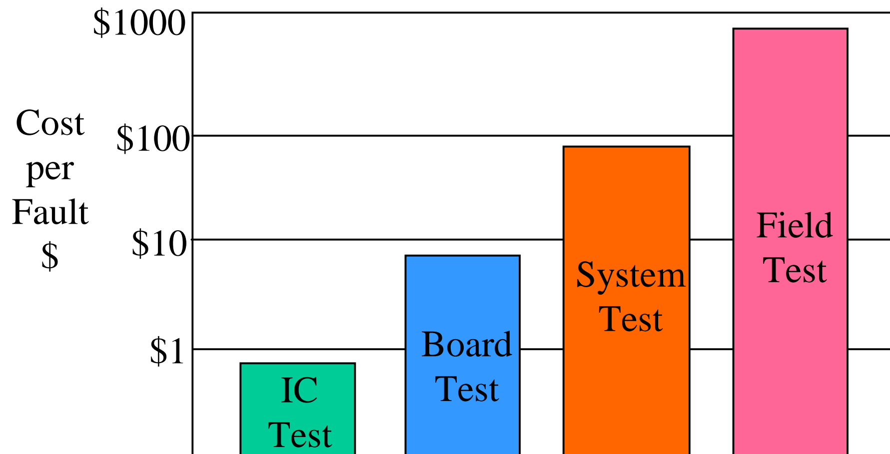
- Circuit complexity is increasing
  - ⇨ more than 2 million transistors/chip is common
  - ⇨ embedded cores ⇒ chips ⇒ MCMs ⇒ boards ⇒ systems
  - ⇨ mixed-signal chips and systems (digital & analog)
  - ⇨ new technologies introduce new kinds of faults
- Risk of manufacturing/fabrication defects is increasing
  - ⇨ larger die size: more area ⇒ more defects
  - ⇨ smaller feature size: thinner & closer lines ⇒ more opens/shorts
  - ⇨ new defect models: closer lines ⇒ more cross-talk
  - ⇨ higher performance: more critical paths ⇒ more delay faults

The Testing Problem (cont.)

- Test accessibility is decreasing
  - ⇨ ICs have more gates & fewer pins
    - ⊙ pin count increased 1 order of magnitude in 20 years
    - ⊙ transistor count increased 5 orders of magnitude in 20 years
  - ⇨ 2-sided surface-mount components & multi-layer PCBs
    - ⊙ in-circuit testing is no longer feasible
- Cost of developing tests is increasing
  - ⇨ ***Dataquest***: 22% (1988) ⇒ 40% (today) of chip dev. cost
    - ⊙ manual test development requires 12-24 people-months
  - ⇨ Algorithmic complexity of test CAD tools (n = # gates)
    - ⊙ fault simulation = $O(n^2)$ vs. ATPG = $O(n^3)$
    - ⊙ "classical" fault models are no longer accurate
      - ↳ accurate fault models difficult to simulate/emulate

The Testing Problem (cont.)

- Automatic Test Equipment (ATE) cost is increasing
  - ⇨ production ATE to test a $50 VLSI chip > $1M
    - ⊙ ***Sematech*** predicts chip tester in 2010 will cost ~ $20M
  - ⇨ at-speed testing needs more expensive ATE
- Product testing goes on long after design is complete
  - ⇨ cumulative testing cost must be considered
  - ⇨ cost of fault location/identification and repair



Note:
Sun Microsystems
claims multiplier > 10
for complex systems

Other Testing Issues & Terminology

- Test stimuli source:
  - ⦿ internal - ***self-testing***
  - ⦿ test machine - ***external testing***
- Signals used for test:
  - ⇨ only I/O signals
    - ⦿ devices – ***I/O pin testing***
    - ⦿ PCBs - ***edge-connector testing***
  - ⇨ I/O and internal signals
    - ⦿ PCBs only - ***bed-of-nails testing, in-circuit testing***
- Speed of test application:
  - ⦿ slower than normal operation - ***static testing***
  - ⦿ at normal operation speed - ***at-speed testing***

Other Testing Issues & Terminology (cont.)

- Output response analysis
  - ⇨ look at the complete output response *R*
    - ⊙ larger memory requirements to store all output responses
  - ⇨ look at a compressed response *f*(*R*) - ***compacted testing***
    - ⊙ higher probability of faulty circuits escaping detection
- Checking the output response:
    - ⊙ the system checks itself - ***self-testing***
    - ⊙ a test machine - ***external testing***
- Type of output responses checked:
    - ⊙ logic values - ***logic testing***
    - ⊙ output response time (set-up/hold time) - ***speed testing***
    - ⊙ I/O voltages & currents - ***parametric testing***
    - ⊙ power supply current – I_{DDQ} ***or*** I_{DDt} ***testing***

Other Testing Issues & Terminology (cont.)

- System level testing:
  - ⊙ concurrent with normal operation - ***on-line testing***
  - ⊙ while system is out-of-service - ***off-line testing***
- Test sequence:
  - ⊙ fixed, always apply same test - ***pre-computed testing***
  - ⊙ dynamic, based on test results thus far - ***adaptive testing***
- Ultimate goal of test:
  - ⇨ ***Quality***: # defective products shipped to customers?
  - ⇨ ***Quality target***: typically < 100 DPM (Defects Per Million)
  - ⇨ But how do we evaluate and ensure the quality?