

## **ELEC 5250/6250 Assignment #6**

Develop a VHDL model for the Mixed-Signal Built-In Self-Test to meet the specifications given in revision 3 of the project description. Simulate, debug, and verify your VHDL model. Email your VHDL model to the instructor before the beginning of class on the day the assignment is due. The grade for this assignment will be based on your model's ability to meet specifications as stated in the revision 3 description and as determined the instructor's independent simulation stimuli. Therefore, it is imperative that you do a thorough job of design verification which includes developing an effective set of input stimuli of your own. Synthesize your final design using Leonardo for: 1) a Spartan II FPGA and 2) AMI 0.5 $\mu$ m CMOS standard cell library. Record or print your synthesis results in terms of:

For Spartan II FPGA:

- 1) number of IOs used
- 2) number of Function Generators used (this is the number of 4-input LUTs used)
- 3) number of CLB slices used (recall there are 2 slices per PLB in the Spartan II)
- 4) number of DFFs or latches used
- 5) maximum clock frequency

For AMI 0.5 $\mu$ m CMOS standard cells (use typical processing):

- 1) list of standard cells used (cell column)
- 2) number of uses of each cell (references column)
- 3) total area (in gates) of each cell (total area column)
- 4) total area in gates (total accumulated area number)
- 5) maximum clock frequency

Turn in your synthesis results on paper at the beginning of class on the day the assignment is due. Extra credit points will be given to the most efficient synthesis in terms of area (LUTs/FFs for FPGA, and total area in gates for standard cell) that meets all specifications. Awards will be for 1<sup>st</sup>, 2<sup>nd</sup>, and 3<sup>rd</sup> place in graduate and undergraduate student categories where ties split the extra credit points.