

ELEC 5250/6250 Assignment #5

Use the ASL description for the ISCAS benchmark circuit assigned to you (get the ASL for circuit assigned to you from my bin directory `~strouce/bin/iscas`); this circuit will be used for all of this assignment. The assigned circuits are listed on the last page of this assignment.

Part 1. Random Test Patterns

Generate 2000 random test patterns for your circuit using the random vector generator I have prepared for you and placed in my bin directory. To access this program from UNIX type the following:

```
~strouce/bin/ranvec s#.vec 2000 #ins
```

where *s#* is the name of your assigned circuit and *#ins* is the number of primary inputs to your circuit (not counting the clock input). Make sure your vector set *s#.vec* matches your ASL file prefix name *s#.asl*.

Make a dummy library file (an empty file or a file with just a valid AUSIM comment: *# comment ;*) named *s#.lib*. Run a parallel fault simulation using the workstation version of AUSIM for both collapsed and uncollapsed single stuck-at gate-level faults and run a serial fault simulation for collapsed faults only. Record the time required for each simulation. Use the following control files for you parallel fault simulations:

For collapsed faults:

default *s#*
proc
audit
simul8
fltgen
pftsim

For uncollapsed faults:

default *s#*
proc
simul8
uncol
fltgen
pftsim

For your serial fault simulation use the command *fltsim* instead of the *pftsim* command in the control file for collapsed faults. Record the following data for your circuit (this info will be in *s#.aud*):

Total number of primary inputs (not counting the clock input)
Total number of primary outputs
Total number of gates
Total number of gate I/O

Record (or calculate) the following data for each of your circuit serial (collapsed faults only) and parallel fault simulations (for both collapsed & uncollapsed faults):

Total number of faults (these faults will be in *s#.flt*):
Number of faults detected (these faults will be in *s#.det*):
Number of undetected faults (these faults will be in *s#.udt*):
Number of potentially detected faults (these faults will be in *s#.pdt*):
Fault simulation time
(you can look at the time-date stamp on *s#.out* for the start time and look at the later time of *s#.det* and *s#.udt* for the end time):
Fault coverage:
Did all primary outputs initialize (look at simulation results in *s#.out*)?

Part 2. Random Scan Patterns

Generate 200 random test patterns for scan design testing of your circuit using the random vector generator but this time we will use some additional options to generate scan vectors. Note that there are no scan flip-flops in your circuit but AUSIM can simulate your circuit as if scan design were implemented (but without the shifting in of the test vectors so the simulation should be fairly fast – only one of the many reasons why AUSIM is awesome). To access this program from UNIX type the following:

```
~strouce/bin/ranvec s#.vec 200 #ins scan #ffs
```

where *s#* is the name of your assigned circuit, *#ins* is the number of primary inputs to your circuit (not counting the clock input), and *#ffs* is the number of DFFs in your circuit. You can get the number of flip-flops in your circuit from the comments at the beginning of the ASL file or by first generating the scan chain file for your circuit by typing:

```
~strouce/bin/cbistext s#.csl s#.scn
```

The *s#.scn* file generated by this command will be needed by AUSIM for your scan chain flip-flop ordering during the simulation (so you will have to do this step anyway). Make sure your scan chain file *s#.scn* and your vector set *s#.vec* matches your assigned *s#.asl* file prefix name. Run parallel fault simulations with the workstation version of AUSIM for both collapsed and uncollapsed single stuck-at gate-level faults and record the time required for each simulation. Use the following control files for you parallel fault simulations:

For collapsed faults:

default *s#*
proc
simul8
fltgen
pftsim

For uncollapsed faults:

default *s#*
proc
simul8
uncol
fltgen
pftsim

Record (or calculate) the following data for each of your circuit parallel fault simulations:

Number of flip-flops in your circuit:

Total number of faults (these faults will be in *s#.flt*):

Number of faults detected (these faults will be in *s#.det*):

Number of undetected faults (these faults will be in *s#.udt*):

Number of potentially detected faults (these faults will be in *s#.pdt*):

Fault simulation time

(you can look at the time-date stamp on *s#.out* for the start time and look at *s#.det* or *s#.udt* for the end time):

Fault coverage:

Did all primary outputs initialize (look at simulation results in *s#.out*)?

Turn in the specified results (from the five fault simulations) on paper at the beginning of class on Thursday November 18. **Be sure** to include your *s#* on the sheet of paper. See the next page for the list of assigned circuits.

Circuit	Name
S499	Jody Burrows
S386	James Corder
S510	Jimmy Duggan
S208	Lonnie Hill
S298	Jonathan Kilpatrick
S635	Joseph Moore
S382	James Thorton
S420	Lisandro Valle
S344	Sukho Yoon
S1269	Sachin Dhingra
S1423	Srinivas Garimella
S953	Ramraj Gottiparthi
S713	Hillary Grimes
S641	Kyung Hwan Han
S1512	Jonathan Harris
S3271	Vasanth Kakani
S838	Jithendra Palasagaram
S967	John Sunwoo
S820	Sudheer Vemula
S3384	Dayu Yang
S3330	Xuefeng Yu