ELEC 5250/6250 Assignment #4

Correct any mistakes in (and re-simulate as needed) your VHDL model from Assignment #3 for an *N*-bit, rising edge-triggered, internal feedback Linear Feedback Shift Register (LFSR) with programmable characteristic polynomial (POLY) and an active high synchronous preset (PRE). The outputs of the LFSR are the *N* flip-flop outputs (LFSR). Synthesize your VHDL model using *Leonardo* with a default value of *N*=8 for: 1) a Xilinx Spartan II FPGA and 2) for AMI 0.5μm CMOS standard cells. (See overview below for notes on Leonardo synthesis) Turn in a print out of your VHDL model and your synthesis results for your working model. The synthesis results should include:

For Spartan II FPGA:

1) number of IOs used
2) number of Function Generators used (this is the number of 4-input LUTs used)
3) number of CLB slices used (recall there are 2 slices per PLB in the Spartan II)
4) number of DFFs or latches used
5) maximum clock frequency

For AMI 0.5μm CMOS standard cells (use typical processing):

1) list of standard cells used (cell column)
2) number of uses of each cell (references column)
3) total area (in gates) of each cell (total area column)
4) total area in gates (total accumulated area number)
5) maximum clock frequency

A Quick Overview of *Leonardo*
(for those of you who missed Dr. Nelson's lecture)

1. On the UNIX system go to your working Mentor directory and type in: *leonardo*
2. In the Quick Setup window select the desired technology for synthesis (FPGA-Xilinx-Spartan2 or ASIC-ADK-AMI 0.5 micron (typ)
3. Open your VHDL source file
4. Run Flow
5. Synthesis results will appear in the Transcript Window (this is where you get the synthesis results specified for the assignment but this info will also be written in the *.sum* file for FPGA and *.log* file for standard cell)
6. Use the View RTL/Technology/Critical Path Schematic buttons on the tool bar to see the schematic results of your synthesis in each technology
7. Note that the standard cell synthesis will produce a structural VHDL file of the standard cells used while the FPGA synthesis will produce an *.edf* file (used by Xilinx ISE tools to perform place and route as well as configuration bit file generation)

Hint: you might want to get out of Leonardo between synthesis sessions for FPGA and standard cell.