Embedded Processors in Xilinx FPGAs

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FPGA Architectures

- **4000/Spartan**
  - $N \times N$ array of unit cells
  - Unit cell = CLB + routing
    - Special routing along center axes
  - I/O cells around perimeter

- **Virtex/Spartan-2**
  - $M \times N$ array of unit cells
  - Added block 4K RAMs at edges

- **Virtex-2/Spartan-3**
  - Block 18K RAMs in array
  - Added 18x18 multipliers with each RAM
  - Added PowerPCs in Virtex-2 Pro

- **Virtex-4/Virtex-5**
  - Added 48-bit DSP cores w/multipliers
  - I/O cells along columns for BGA
Xilinx Virtex-4 FPGAs

- Configuration memory: 4.7M to 50.8M bits of RAM
- PLBs: 1,536 to 22,272
  - 4 slices per PLB
    - 2 LUTs & 2 FFs per slice
    - 2 slices can operate as RAMs/SRs
- Block RAMs: 48 to 552 18K-bit dual-port RAMs
  - Also operate as FIFOs
- DSP cores: 32 to 512, each includes:
  - 18x18-bit multiplier
  - 48-bit adder & accumulator
- Up to 2 PowerPC processors
Embedded Processors

- **Hard core**
  - Faster
  - Fixed position
  - Few devices

- **Soft core**
  - Slower
  - Can be placed anywhere
  - Applicable to many devices

**Virtex-4 Processors:**

<table>
<thead>
<tr>
<th>Embedded Processor</th>
<th>Core Type</th>
<th>Max Clock Frequency</th>
<th>Slices</th>
<th>PLBs</th>
<th>Block RAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PowerPC</td>
<td>Hard</td>
<td>222 MHz</td>
<td>1000</td>
<td>250</td>
<td>9</td>
</tr>
<tr>
<td>Microblaze</td>
<td>Soft</td>
<td>180 MHz</td>
<td>940</td>
<td>235</td>
<td>9</td>
</tr>
<tr>
<td>Picoblaze</td>
<td>Soft</td>
<td>221 MHz</td>
<td>333</td>
<td>84</td>
<td>3</td>
</tr>
<tr>
<td>Picoblaze (optimized)</td>
<td>Soft</td>
<td>233 MHz</td>
<td>274</td>
<td>69</td>
<td>3</td>
</tr>
</tbody>
</table>
Specialized Cores

Virtex and Spartan II

Virtex II and Spartan 3

4K-bit RAMs

18K-bit RAMs and 18×18-bit multipliers

RAMs/multipliers
Programmable RAMs

- 18 Kbit dual-port RAM
- Each port independently configurable as
  - 512 words x 36 bits
    - 32 data bits + 4 parity bits
  - 1K words x 18 bits
    - 16 data bits + 2 parity bits
  - 2K words x 9 bits
    - 8 data bits + 1 parity bit
  - 4K words x 4 bits (no parity)
  - 8K words x 2 bits (no parity)
  - 16K words x 1 bit (no parity)

- Each port has independently programmable
  - clock edge
  - active levels for write enable, RAM enable, reset
Specialized Cores

- 18K bit RAMs
- Xtreme DSPs

Cores

- 4VLX15
- 4VLX25
- 4VLX40
- 4VLX60
- 4VLX80
- 4VLX100
- 4VLX160
- 4VLX200
- 4VSX25
- 4VSX35
- 4VSX55
- 4VFX12
- 4VFX20
- 4VFX40
- 4VFX60
- 4VFX100
- 4VFX140

Virtex 4

Embedded Systems
Spartan-6 DSP Architecture

- All DSP slices identical
  - 16-120 DSPs in 1-4 cols
- Each DSP includes:
  - 18x18-bit 2's-comp multiplier (w/ adder)
  - 2-input, 48-bit adder/subtractor
    - P = Z±X+Cin
  - 18-bit adder/subtractor
    - B1 = D±B
  - User controlled operational modes
    - For X & Z MUXs
    - Pre-adder MUX
  - Configuration bits control
    - Pipeline register MUXs
    - Active levels of Resets and Clock Enables

Cascade outputs w/ dedicated routing:
- Bcout(18) Ccout(1) Pcout(48)

Cascade inputs from dedicated routing:
- Bcin(18) Pcin(48) Cin(1)