

Example ADDER with concatenation operator for carry

```
library ieee;
use ieee.std_logic_1164.all;
use work.std_arith.all;
entity ADDER is
generic (N: integer := 4);
port (A,B: in std_logic_vector(N-1 downto 0);
      Cin: in std_logic;
      S: out std_logic_vector(N-1 downto 0);
      Cout: out std_logic);
end entity ADDER;
architecture RTL1 of ADDER is
begin
process (A,B,Cin)
variable C: std_logic_vector(N downto 0);
begin
    C := ('0' & A) + ('0' & B);
    if (Cin = '1') then
        C := C + 1;
    end if;
    for i in 0 to N-1 loop
        S(i) <= C(i);
    end loop;
    Cout <= C(N);
end process;
end architecture RTL1;
```

Example ADDER for controlling synthesis

```
library ieee;
use ieee.std_logic_1164.all;
entity ADDER is
generic (N: integer := 4);
port (A,B: in std_logic_vector(N-1 downto 0);
      Cin: in std_logic;
      S: out std_logic_vector(N-1 downto 0);
      Cout: out std_logic);
end entity ADDER;
architecture RTL2 of ADDER is
begin
process (A,B,Cin)
variable C: std_logic_vector(N downto 0);
begin
    C(0) := Cin;
    for i in 0 to N-1 loop
        S(i) <= A(i) xor B(i) xor C(i);
        C(i+1) := (A(i) and B(i)) or
                  (A(i) and C(i)) or
                  (B(i) and C(i));
    end loop;
    Cout <= C(N);
end process;
end architecture RTL2;
```

Example ADDER using function

```

entity ADDER is
generic (N: integer := 4);
port (A,B: in bit_vector(N-1 downto 0);
      Cin: in bit;
      S: out bit_vector(N-1 downto 0);
      Cout: out bit);
end entity ADDER;
architecture RTL3 of ADDER is
signal C: bit_vector(N downto 0);
function FA_SUM (AI,BI,CI: bit) return bit is
begin
    return AI xor BI xor CI;
end function FA_SUM;
function FA_CARRY (AI,BI,CI: bit) return bit is
begin
    return (AI and BI) or (AI and CI) or (BI and CI);
end function FA_CARRY;
begin
process (A,B,Cin)
begin
    C(0) <= Cin;
    for i in 0 to N-1 loop
        S(i) <= FA_SUM(A(i),B(i),C(i));
        C(i+1) <= FA_CARRY(A(i),B(i),C(i));
    end loop;
    Cout <= C(N);
end process;
end architecture RTL3;

```

COMBINATIONAL LOGIC MODELING & SYNTHESIS

RTL1

```
-- default synthesis (exhaustive & speed)
-- Utilization          N=4  71/446      N=8 no synthesis
-- Total PIN signals    22/ 70
-- Macrocells Used     20/128
-- Unique Product Terms 157/640
-- for N:=4, synthesis options (exhaustive & area)
-- Utilization          67/446      N=8 no synthesis
-- Total PIN signals    16/ 70
-- Macrocells Used     18/128
-- Unique Product Terms 156/640
-- for N:=4, synthesis options (normal & area)
-- Utilization          69/446      N=8 no synthesis
-- Total PIN signals    20/ 70
-- Macrocells Used     18/128
-- Unique Product Terms 170/640
-- for N:=4, synthesis options (none & area) N=8 N=12 N=16 N=20
-- Utilization          63/446      123  179  230  269
-- Total PIN signals    21/ 70      38   56   67   70
-- Macrocells Used     25/128      47   69   91  113
-- Unique Product Terms 63/640      133  203  273  343
```

RTL2

```
-- default synthesis (exhaustive & speed)
-- Utilization          N=4  48/446      N=8 no synthesis
-- Total PIN signals    16/ 70
-- Macrocells Used     13/128
-- Unique Product Terms 125/640
-- for N:=4, synthesis options (exhaustive & area)
-- Utilization          48/446      N=8 no synthesis
-- Total PIN signals    16/ 70
-- Macrocells Used     13/128
-- Unique Product Terms 125/640
-- for N:=4, synthesis options (normal & area)
-- Utilization          48/446      N=8 no synthesis
-- Total PIN signals    16/ 70
-- Macrocells Used     13/128
-- Unique Product Terms 170/640
-- for N:=4, synthesis options (none & area) no synthesis
```

COMBINATIONAL LOGIC MODELING & SYNTHESIS

RTL3

```
-- default synthesis (exhaustive & speed)           N=8
-- Utilization                N=4  48/446           215
-- Total PIN signals          16/ 70              35
-- Macrocells Used            13/128              48
-- Unique Product Terms       125/640            609
-- for N:=4, synthesis options (exhaustive & area) N=8
-- Utilization                48/446           215
-- Total PIN signals          16/ 70              35
-- Macrocells Used            13/128              48
-- Unique Product Terms       125/640            609
-- for N:=4, synthesis options (normal & area)      N=8
-- Utilization                48/446           215
-- Total PIN signals          16/ 70              35
-- Macrocells Used            13/128              48
-- Unique Product Terms       125/640            609
-- for N:=4, synthesis options (none & area) N=8 N=12 N=16 N=20 N=22
-- Utilization                29/446           57  85  113  141  155
-- Total PIN signals          14/ 70           26  38   50   62   68
-- Macrocells Used            8/128            16  24   32   40   44
-- Unique Product Terms       28/640           56  84  112  140  154
```