

# Simulation and Synthesis of a Stored Program Computer Architecture

- Simulate an example program for PicoBlaze
- Write a PicoBlaze assembly language program to perform hexadecimal to 7-segment display conversion
- Simulate, debug, and verify the operation of your design
- Download, debug and verify the operation of your program on the Spartan 3 FPGA

# PicoBlaze Microcontroller

- Pre-Lab exercise:
  - Read the PicoBlaze User's Guide Chapters 10-12 (19 pages)
  - Read the PicoBlaze tutorial (3 pages)
  - Study PicoBlaze architecture and instruction set
  - Write an assembly language program for PicoBlaze to implement a hexadecimal to 7-segment decoder with
    - HEX input IN\_PORT
    - 7-segment data on OUT\_PORT

# PicoBlaze Microcontroller

- Lab exercise:
  - Download & extract the PicoBlaze.zip file from class web page
    - Simulate tutorial.psm program using pBlazeIDE and assemble program using KCPSM2
    - Synthesize and download PicoBlaze with assembled tutorial.psm program with input port connected to switches and output port connected to LEDs
    - Record the number of slices from the synthesis report
    - Demonstrate synthesized circuitry to GTA
  - Simulate and debug your PicoBlaze program for hex-to-7segment decoder via pBlazeIDE
    - Assemble, synthesize, and download your PicoBlaze based decoder on Spartan 3 PCB
    - Demonstrate synthesized circuitry to GTA

# PicoBlaze Microcontroller

- Note: increasing the number of “output” instructions will increase the brightness of the display
- An alternate approach is to include a latch or register enabled by the PicoBlaze `WRITE_STROBE` to hold the 7-segment values
  - You can include a level-sensitive latch, or
  - Your parallel load register from Lab#5

# PicoBlaze Microcontroller

Post-lab assignment:

- Lab report should include:
  - A description of your assembly language program and how it works
  - Your PicoBlaze program(s) should be included
  - A description of the design verification simulation you did
  - A discussion of the synthesis, and download to the FPGA
    - What went right and wrong in your design and program
- Lab report is due at beginning of the next lab session