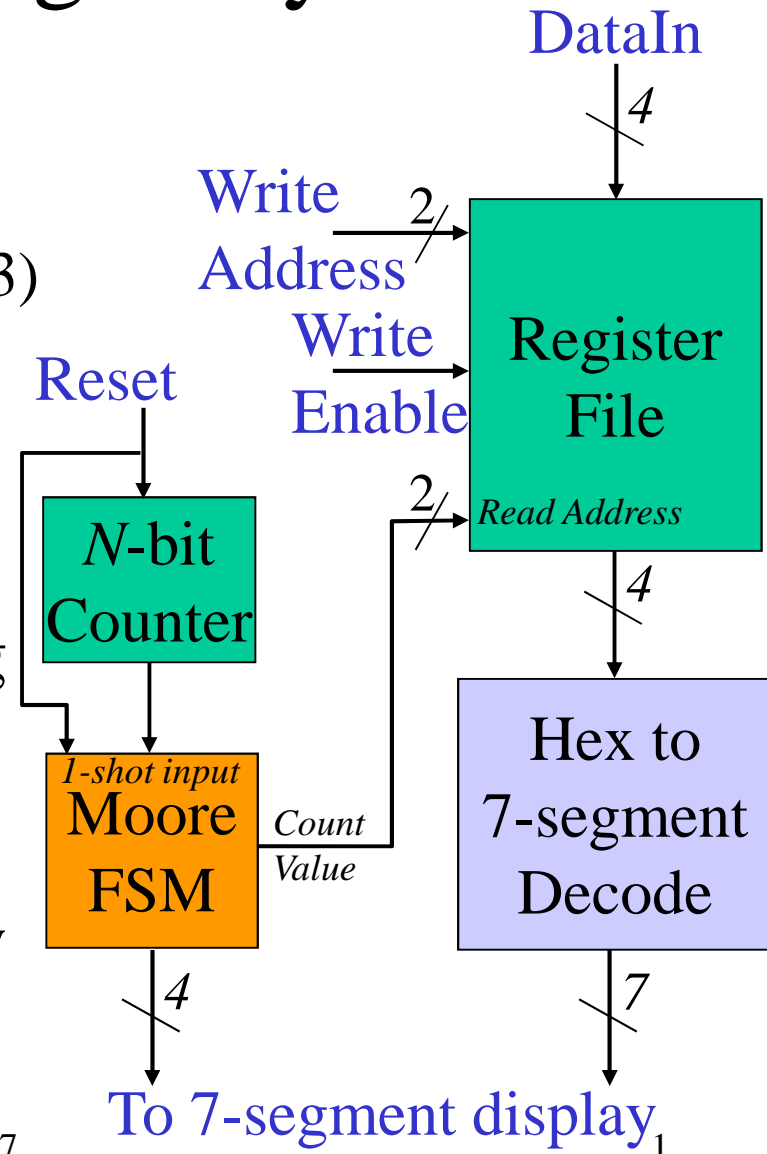


Hierarchical Modeling & Synthesis

- Write a top-level VHDL to combine your models for
 - Hex to 7-segment decoder (Lab#3)
 - Moore FSM (Lab#4)
 - Register File (Lab#6)
 - N-bit counter (Lab#5)
- Simulate and verify (debugging where needed) design using ModelSim
- Synthesize, download, & verify design in Spartan 3 FPGA



Time-Multiplexed Display

- The overall circuit will time-multiplex control and display data to the four 7-segment displays on the Spartan 3 PCB
- Specifications for design:
 - Hex to 7-segment decoder will convert value read from the register file and supplies A-G values to 7-segment display
 - Register file will take write address, data, and write enable inputs from switches (address & data) and push button (write enable)
 - N -bit counter MSB will supply the digital one-shot input clock enable to the FSM to advance the FSM once every 2^N clock cycles
 - Use the parameterized register/counter with inputs tied to values such the counter always counts
 - ✓ Determine these values as part of your pre-lab
 - Moore FSM will supply
 - Active low enables (AN0-3) to 7 segment display to cycle through 4 displays
 - ✓ Let S0 drive AN0, S1 drive AN1, and so on
 - Read address (count value) to register file
 - Clock input to FSM and N -bit counters will come from oscillator

Time-Multiplexed Display

- Pre-lab assignment:
 - Write the top level VHDL description for your design using the previous models as components
 - Set the logic values to the input of the register/counter to obtain the N -bit counter
 - Determine the FPGA pin numbers for register file inputs
 - ✓ Address and Data inputs from DIP switches
 - ✓ Write Enable from Push Button
 - Read “Adding Probes in FPGA Editor” from class web page

Time-Multiplexed Display

- Lab exercise:
 - Show your pre-lab work to the GTA at the beginning of the lab session
 - Simulate your VHDL models and verify your design using ModelSim, debug as necessary
 - Use the Register File generic values $M=2$, $N=4$ for design verification
 - Synthesize your design for the Spartan 3S200 FPGA using ISE
 - Set synthesis options to “Keep Hierarchy” (see next page)
 - ✓ This will help with probing internal nodes for debugging
 - For the N -bit counter use $8 \leq N \leq 25$ and try a couple different values
 - ✓ You can see the display cycling with a larger number (for debugging)
 - Open the synthesis report file and record #Slices, #LUTs, and #FF/latches for each value of N used for the counter
 - Open FPGA Editor and verify the #Slices used
 - Test and debug your circuit using the PCB functions
 - Add probes in FGPA Editor as needed for debugging
 - Demonstrate your working circuit to the GTA

Controlling Synthesis Options

- In processes window, right click “Synthesis” and select “Properties”
 - Under “Property Display Level” select “Advanced”
 - There are three “options” windows
 - Synthesis Options
 - ✓ Controls optimization target and effort
 - » area vs performance
 - ✓ Keep Hierarchy = Yes maintains many VHDL signal names
 - HDL
 - ✓ Controls extraction of RAMs and shift registers
 - Xilinx Specific
 - ✓ Controls use of clock enables, set/reset

Time-Multiplexed Display

- Post-lab: Turn in your lab report at the beginning of the next lab session, including:
 - Verified parameterized VHDL model
 - Simulation results
 - Synthesis Report results (#slices, #LUTs, and #FFs/latches)
 - Number of slices found in FPGA Editor
 - The value of N you used for the counter
 - Pre-lab work, including
 - FPGA pin numbers and PCB functions used for synthesis

Dim and/or Bleeding Display?

- Add an 11-bit register on the output
 - For 7-segment values and 4 enable values
 - Register is enabled by output of 1-shot
- The holds the outputs active for the maximum amount of time until the next value is ready to display with good brightness and minimum bleeding across digits