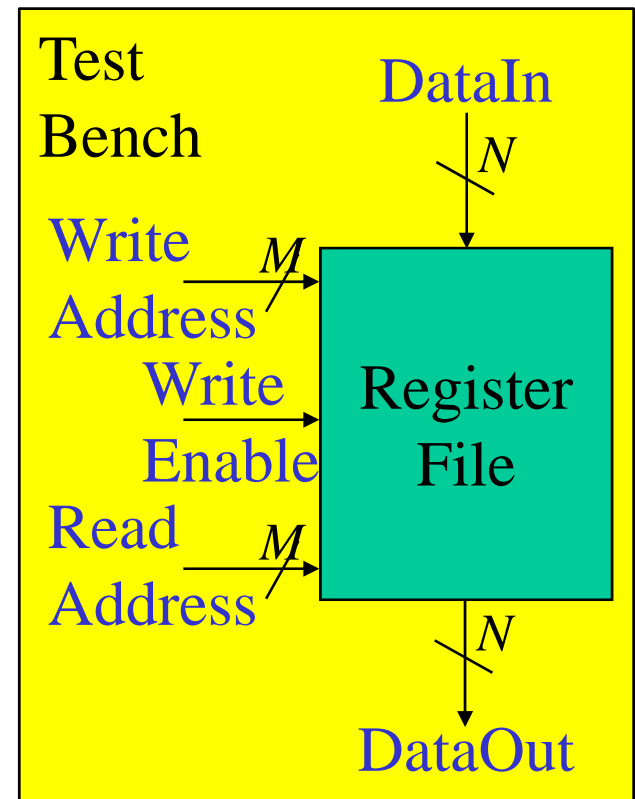


Parameterized VHDL Modeling & Synthesis of Register File w/Test Bench

- Write a parameterized VHDL model for a Register File
 - See next page for specifications
- Simulate and verify (debugging where needed) design using ModelSim
- Synthesize and download design into Spartan 3 FPGA



Parameterized Register File

- A register file is like a small RAM
- Specifications for parameterized register file:
 - 2^M registers of N -bits each
 - M write address bits & an active high write enable
 - when write enable is active, contents of register selected by write address = Data inputs
 - ✓ Note that these are level sensitive latches
 - M read address bits
 - Data outputs = contents of register selected read address

Parameterized Register File

- Pre-lab assignment:
 - Write:
 - VHDL description for design with specifications on previous page
 - VHDL hierarchical parameterized test bench to call up register file model and apply algorithm on following page
 - Determine the FPGA pin numbers for
 - Assuming $M=2$ and $N=4$
 - ✓ Address and Data inputs from DIP switches
 - ✓ Write Enable from push button
 - ✓ Data outputs to the LEDs
 - » You will use these to test your design on Spartan 3 PCB
 - Read from class web page
 - “Overview of FPGA Editor”
 - “Adding probes in FPGA Editor”

Test Bench Algorithm

1. $\uparrow\downarrow$ (write address as data)
2. \uparrow (read address, write inverted address as data)
3. \downarrow (read address, write address as data)
4. \uparrow (read address)

\uparrow = indicates ascending addresses

\downarrow = indicates descending addresses

$\uparrow\downarrow$ = indicates addressing in either direction

Parameterized Register File

- Lab exercise:
 - Show your pre-lab work to the GTA at the beginning of the lab session
 - Simulate your VHDL test bench and model and verify your design using ModelSim, debug as necessary
 - Use the values $M=3, N=3$ and $M=2, N=4$ for simulation design verification
 - Be sure to apply adequate set-up and hold time on data and address for the level-sensitive latches
 - Synthesize your VHDL register file model (not the test bench) for the Spartan 3S200 FPGA using ISE
 - Use the values $M=2, N=4$ for synthesis
 - Open the synthesis report file and record #Slices, #LUTs, and #FF/latches
 - Open FPGA Editor and verify the #Slices used
 - While in FPGA Editor, add probes to a full word in the register file
 - ✓ Bring probe bits out to LEDs or segments of the 7-segment display
 - Test and debug your circuit using the PCB functions (i.e., switches, LEDs, etc.)
 - Demonstrate your working circuit to the GTA
 - ✓ Including the probed bits

Parameterized Register File

- Post-lab: Turn in your lab report at the beginning of the next lab session, including:
 - Verified parameterized VHDL model
 - Verified VHDL test bench
 - Simulation results for different values of N & M
 - Synthesis Report results (#slices, #LUTs, and #FFs/latches)
 - Number of slices found in FPGA Editor
 - Pre-lab work, including
 - FPGA pin numbers and PCB functions used for synthesis