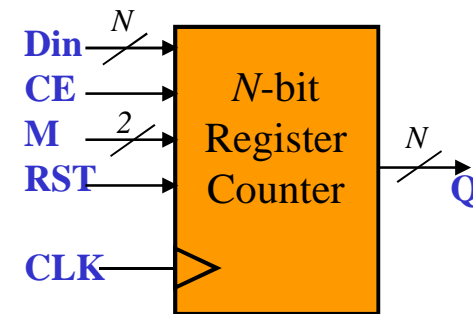


Hierarchical & Parameterized VHDL

Modeling, Simulation & Synthesis

- Write a parameterized VHDL model for a rising edge-triggered N -bit universal register/counter with following specifications (in order of precedence):

- Active high reset (RST)
- Active high clock enable (CE)
- Two mode control inputs (M1 & M0)
- See function table for modes of operation



- Simulate & verify design for at least 2 different values of N
- Synthesize, download & verify multiple implementations of design in Spartan 3 FPGA
- Note: during shift register mode $Q_{n-1} \leq D_{n-1}$

RST	CE	M1	M0	Q^+	Function
1	X	X	X	$Q_i^+ \leq 0$	Reset
0	1	0	0	$Q^+ \leq Q$	Hold
0	1	0	1	$Q_i^+ \leq Q_{i+1}$	Shift
0	1	1	0	$Q^+ \leq Q+1$	Count
0	1	1	1	$Q^+ \leq Din$	Load

Parameterized VHDL Register/Counter

- Pre-lab assignment:
 - Write a parameterized VHDL for the register/counter using the specifications on the previous page
 - Write a separate VHDL model for the digital one-shot from Lab#4
 - Write a hierarchical VHDL model that calls and connects the register/counter model and the digital one-shot model
 - Where the output of the digital one-shot drives the clock enable (CE)
 - Determine the values of N you will use for simulation and design verification
 - Explain why you are choosing these values?
 - Determine the FPGA pin numbers you will use for LEDs, push buttons, and/or switches during operation in the FPGA for the various values of N
 - Make a table of these pin numbers and their function

Parameterized VHDL Register/Counter

- Lab exercise Part 1:
 - Show your pre-lab work to the GTA at the beginning of the lab session
 - Simulate and verify your register/counter VHDL design
 - Use at least two different values of N & debug as necessary
 - Simulate and verify your hierarchical model that calls the register/counter and the digital one-shot
 - Synthesize your design for the Spartan-3 PCB using your input pin and output pin assignments
 - Record the number of flip-flops (FFs), LUTs, and slices used
 - Test your circuit using the PCB LEDs, switches, and/or push buttons
 - Demonstrate your working circuit
 - Repeat the exercise with a different value of N
 - Record the number of flip-flops (FFs), LUTs, and slices used

Parameterized VHDL Register/Counter

- Lab exercise Part 2:
 - For each of the following circuits, modify your hierarchical VHDL model, synthesize, download and verify your design for the Spartan-3 PCB using your input pin and output pin assignments
 - Record the number of flip-flops (FFs), LUTs, and slices used
 - Also record the value of N used in the design
 - Circuit #1 – counter (tie $M1=1$ and $M0=0$)
 - Circuit #2 – shift register (tie $M1=0$ and $M0=1$)
 - Circuit #3 – parallel load register (tie $M1=1$ and $M0=1$)
 - Note that RST and CE must still work on all three circuits
 - Demonstrate your working circuits

Parameterized VHDL Register/Counter

- Post-lab: Turn in your lab report at the beginning of the next lab session, including:
 - Verified parameterized VHDL models
 - Simulation results
 - Table of synthesis results
 - for each value of N and each hierarchical implementation
 - ✓ #slices, #LUTs, and #FFs/latches
 - Pre-lab work, including
 - FPGA pin numbers and PCB functions used for synthesis
 - A brief explanation of why you chose the values of N you chose for your design verification