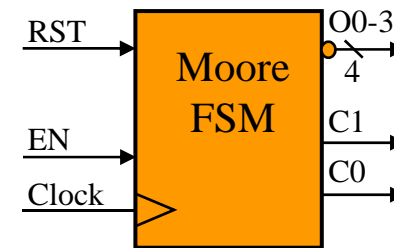


VHDL Modeling & Synthesis

Sequential Logic Design

- Write a VHDL model for the FSM from Lab#2
 - Use the same specifications as Lab #2 *and*
 - Include the digital one-shot in your model
- Simulate and verify design using ModelSim
 - Debug as needed
- Synthesize, download, and verify design in Spartan 3 FPGA

block diagram



VHDL Sequential Logic Design

- Pre-lab assignment:
 - Write a VHDL model for your design using the same specifications as the design for Lab #2
 - Include the digital one-shot in the model
- Read “Overview of FPGA Editor” (3 pages) from lab web page
- Show your pre-lab work to the GTA at the beginning of the lab session

VHDL Sequential Logic Design

- Lab exercise:
 - Simulate your VHDL and verify your design using ModelSim, debug as necessary
 - Synthesize, download, and verify your design in the Spartan 3 FPGA using ISE
 - Open the synthesis report file and record #LUTs, #FF/latches, #slices, and maximum clock frequency
 - Open your design in FPGA Editor and find the two FFs for your FSM, record the logic equations of the LUTs driving these two FFs
 - Demonstrate your working circuit
- *Save your working VHDL model*
 - *It will be used again in later labs*

VHDL Sequential Logic Design

- Lab exercise:
 - Click and run the submenu under Place&Route menu
 - Generate Post-Place&Route Simulation Model
 - Simulate this simulation model
 - The model can be found in the netgen/par subdirectory
 - Compare timing delays to original VHDL simulation
 - These represent the actual FPGA implementation delays
- Post-lab: Turn in your lab report at the beginning of the next lab session
 - Include: verified VHDL models, simulation results, data recorded from synthesis report file, observations from post-place&route timing simulation, and pre-lab work