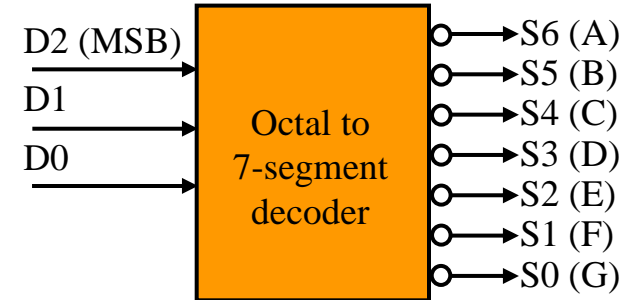


VHDL Modeling & Synthesis of 7-Segment Decoders

- Write a complete VHDL model for an Octal to 7-segment decoder



- Use the same specifications as Lab #1
 - You may use a bit vector for the 7-segment outputs
 - Verify your design through simulation of the VHDL model
 - Synthesize, download & verify the design into Spartan 3 FPGA
- Write a complete VHDL model for a HEX to 7-segment decoder with active low outputs
 - Verify your design through simulation of the VHDL model
 - Synthesize, download & verify the design into Spartan 3 FPGA

VHDL Modeling & Synthesis

- Pre-lab assignment:
 - Write a complete VHDL model for the Octal to 7-segment decoder
 - You may use verified Boolean logic equations from Lab#1, *or*
 - You may use any other valid concurrent or sequential VHDL constructs
 - Read Overview of FPGA Editor on class web page
- Show you Pre-lab work to the GTA at the beginning of the lab session

Lab exercise

- Show your pre-lab work to the GTA at beginning of lab session
- For your Octal to 7-segment decoder VHDL model
 - Verify correct operation of the model via simulation and debug as needed
 - Synthesize model then double click “View Synthesis Report”
 - Record #slices, #LUTs, #FF/latches (see *device utilization summary section*)
 - Open your design in FPGA Editor and find the 7 LUTs
 - Record the logic equation for each LUT from FPGA Editor
 - Download and verify the design in the Spartan 3 FPGA using switches and 7-segment LED display
 - Demonstrate your working decoder to the GTA
- Write a HEX to 7-segment decoder VHDL model
 - *see next page*
- Post-lab: Turn in your lab report at beginning of next lab session
 - Include: verified VHDL models, simulation results, data you recorded from the synthesis report, and pre-lab work

VHDL Modeling & Synthesis of a HEX to 7-Segment Decoder

Write a VHDL model for a Hexadecimal to 7-segment decoder using specifications given below

- Verify your design through simulation of the VHDL model
 - Synthesize, download, & test the design in Spartan 3 FPGA
 - Record #slices, #LUTs, #FF/latches from Synthesis Report
- *Save this VHDL model since it will be used in later labs*

