

# Simulation and Synthesis of a Stored Program Computer Architecture

- Write a VHDL model for the input interface to connect the Boundary Scan port and Shift Register from Lab 8 to PicoBlaze
- Write a hierarchical model to interconnect the following:
  - PicoBlaze with assembled program memory
    - See next page for specifications for assembly language program
  - Boundary Scan port interface circuitry to PicoBlaze
- Simulate, debug, and verify the operation of your design
- Download, debug, and verify the operation of your PicoBlaze architecture and program on the Spartan 3 FPGA

# System Specifications

- Interface circuitry for Boundary Scan to PicoBlaze
  - 6-bit shift register as in Lab 8
    - 6-bit level sensitive latch enabled by BSCAN Update may be used to hold address and data passed to PicoBlaze
  - Also include the MUXs from Lab 8 to assist in debugging
- Interface circuitry for PicoBlaze to 7-segment display
  - 11-bit register enabled by PicoBlaze WRITE\_STROBE is useful to hold 7-segment values plus the display enables
    - Note: only one display enable should be active at a time
- PicoBlaze functional specifications
  - Takes 4-bit HEX data and 2-bit address from BSCAN interface and stores in 1 of 4 registers depending on 2-bit address
    - Note: data for each of the 4 displays can be updated anytime via BSCAN
  - Decodes HEX data to 7-segment display data
  - Passes 7-segment data to display using port ID to enable digit sequence to continuously display 4 independent values

# Advanced Design Options

- Advanced Design
  - In addition to regular system specifications, PicoBlaze displays “ELEC” then “4200” before displaying the 4 BS written 7-segment display values for 4 seconds, then the sequence repeats
- Super Design
  - “ELEC 4200” scrolls across display between displaying the 4 BS written 7-segment display values for 4 seconds

# PicoBlaze Microcontroller

- Pre-Lab exercise (for first lab session):
  - Study PicoBlaze architecture and instruction set
    - Write your PicoBlaze program
    - Note: the brightness of the display of the individual 4 hex digits is a function of how often and how long a given 7-segment display is being driven by the processor, which must be managed in the program
  - Write VHDL models for
    - BS to PicoBlaze interface circuitry
    - PicoBlaze to 7-segment display interface circuitry
    - Top level model to interconnect PicoBlaze and other models

# PicoBlaze Microcontroller

- Lab exercises:
  - Simulate and debug your PicoBlaze program via pBlazeIDE
  - Assemble your verified program via KCPSM3.exe
  - If possible, simulate and verify you top level VHDL model interconnecting all components
  - Synthesize, download, and verify your complete design
  - Demonstrate you complete design to GTA

# PicoBlaze Microcontroller

- Post-lab assignment:
  - Lab report should include:
    - A description of the design you chose (regular, advanced, super) and why
    - A description of the various levels of simulation, synthesis, and download to the FPGA you did and why
    - A discussion of what went right and wrong in your approach to design and design verification
    - A discussion of what you would have done differently if you were starting over with this particular project
    - Your VHDL models and PicoBlaze program(s) should be included in this report and referred to in your discussion
      - ✓ You don't need to turn in the VHDL and PicoBlaze assembly program(s) separately since you are including it in the report
  - Final lab report is due at beginning of lab presentations