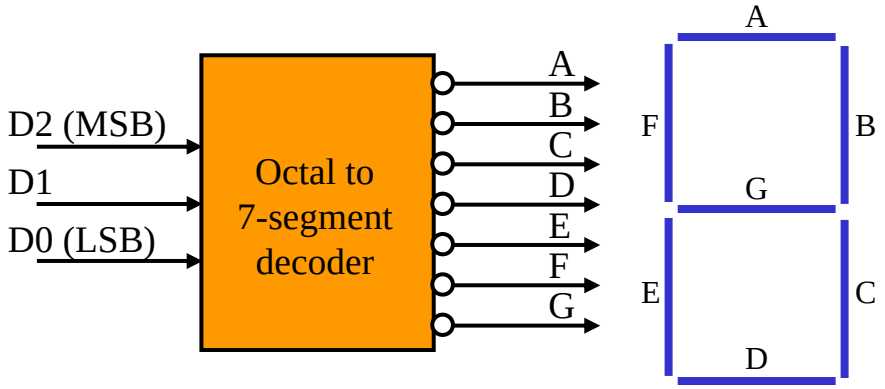
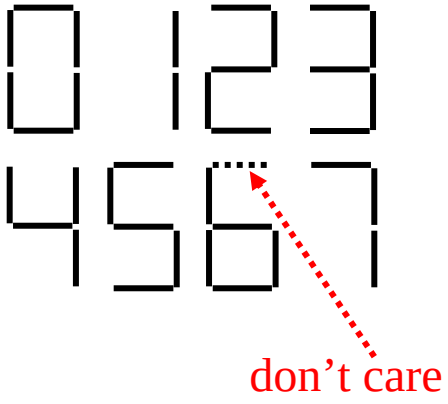
Combinational Logic Design

- Design an octal to 7-segment decoder with active-low outputs (0 turns on LED segment)
  - Inputs: D2-D0
  - Outputs: A-G
- Generate:
  - complete truth table
  - K-maps
  - minimized SOP equations
  - Logic diagram
- Capture schematic, simulate, and verify design (debugging where needed) using Xilinx ISE and Mentor Graphics ModelSim
- Synthesize, download, and verify design onto a Spartan 3 FPGA





Octal to 7-segment Decoder

- Pre-lab assignment:
  - ➢ Drive the Truth Table for the decoder
  - ➢ Use K-maps to obtain minimized SOP expressions
    - Share common product terms and gates where possible
  - ➢ Draw a logic diagram
    - Sharing common gates
    - Label all I/O according to system specifications on page 1
  - ➢ Read the following (available on class web page):
    - ISE Quick Start Guide (pages 24-30)
    - Spartan 3 PCB reference manual
      - ✓ Chapter 1 (4 pages)
      - ✓ Chapter 3 (3 pages)
      - ✓ Chapter 4 (2 pages)

Octal to 7-segment Decoder

- Lab exercise:
  - ➢ Show your pre-lab work to the GTA at the beginning of the lab session
  - ➢ Capture your design using schematic entry
  - ➢ Simulate you circuit for design verification
    - Simulate & verify all possible input values
    - Debug & fix problems if output is incorrect
      - ✓ Check truth table against K-map population
      - ✓ Check K-map groups against logic equation product terms
      - ✓ Check logic equations against schematic

Octal to 7-segment Decoder

- Lab exercise continued:
  - Synthesize your design for the Spartan 3S200 FPGA using ISE
    - Connect inputs (D2-D0) to switches
    - Connect outputs (A-G) to 7-segment display
  - Download and verify your design
    - Debug, re-synthesize, and re-download as needed
  - Demonstrate your working circuit to the GTA
- Post-lab: Turn in your lab report at the beginning of next lab session
  - Be sure follow lab report format in syllabus and include:
    - Printed (or screen capture) copy of your verified schematic and simulation results
    - Your pre-lab work