

ELEC 4200 – DIGITAL SYSTEM DESIGN

(Required for ECPE, Elective for ELEC)

2004 Catalog Data: ELEC 4200. DIGITAL SYSTEM DESIGN (3) LEC. 2. LAB 3. Pr. ELEC 2210 and ELEC 2220. Hierarchical, modular design of digital systems; computer-aided digital system modeling, simulation, analysis, and synthesis; design implementation with programmable logic devices and field programmable gate arrays.

Textbook: VHDL for Programmable Logic, K. Skahill, Addison Wesley, 1996.

References: *VHDL Tutorial & VHDL Design & Simulation with ModelSim EE* Tutorial on line at: <http://www.eng.auburn.edu/department/ee/mgc/mentor.html>

Coordinator: Charles E. Stroud, Professor of Electrical & Computer Engineering

Course Objectives:

- 1. To be able to analyze and design hierarchical digital systems**
- 2. To be able to develop and simulate register-level models of hierarchical digital systems**
- 3. To be able to prototype designs with programmable logic including FPGAs**

Prerequisites by topic:

1. Digital logic design and analysis or switching theory
2. Digital electronics
3. Computer system organization and design

Lecture Topics:

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| 1. Review of digital logic circuit design | (2 classes) |
| 2. CAD tools for design capture & verification | (2 classes) |
| 3. Intro to programmable logic & hardware description languages | (2 classes) |
| 4. Modeling of digital circuits using VHDL | (3 classes) |
| 5. Simulation of digital circuits using VHDL | (2 classes) |
| 6. CAD tools for timing simulation and analysis | (2 classes) |
| 7. Hierarchical design concepts | (2 classes) |
| 8. Hierarchical design using VHDL | (3 classes) |
| 9. Field programmable technologies | (2 classes) |
| 10. Configuration interfaces for field programmable logic | (2 classes) |
| 11. Design using field programmable logic | (2 classes) |
| 12. Boundary Scan interface | (2 classes) |
| 13. Advanced VHDL modeling & modeling guidelines | (2 classes) |
| 14. Exams and project reviews | (4 classes) |

Class schedule (50 minute classes):

Typical methods for evaluating student performance:

Hour quizzes (1)	25%
Final exam	25%
Lab projects	35%
Project presentation	15%

Laboratory Exercises:

1.	Schematic capture & simulation of combinational logic	(1 lab)
2.	Schematic capture & simulation of sequential logic	(1 lab)
3.	Prototyping circuits from labs 1&2 on FPGAs	(1 lab)
4.	VHDL modeling & simulation of digital circuits from labs 1 & 2	(1 lab)
5.	VHDL synthesis of models from lab 4 and synthesis in FPGAs	(1 lab)
6.	VHDL modeling & simulation of an ALU	(1 lab)
7.	VHDL synthesis in FPGAs of ALU from lab 6	(1 lab)
8.	Synthesis options & optimization of ALU	(1 lab)
9.	Hierarchical VHDL modeling & simulation of sequential logic	(1 lab)
10.	VHDL synthesis of hierarchical sequential logic models	(1 lab)
11.	VHDL modeling & simulation of a stored program computer	(2 labs)
12.	VHDL synthesis in FPGAs of stored program computer	(2 labs)

Lab session (3 hours):

Class attendance: Lecture attendance is encouraged, but will not be accounted for in the course grade. Lab attendance is required, and unexcused absences will be accounted for in the course grade.

Policy on unannounced quizzes: There will be no unannounced quizzes.

Special Accommodations: Any student requiring special accommodations should come by the instructor's office within the first two days of class, bringing your letter from the Office of Students with Disabilities.

Contribution of course to meeting the professional component

Engineering topics: 3 credits

33% engineering science (1 credit)

67% engineering design (2 credits)

Primary program outcomes related to this course:

Outcome 1. Ability to apply knowledge of math, science and engineering to solve problems.

Outcome 2. Ability to apply in-depth knowledge in one or more disciplines

Outcome 3. Ability to design an electrical component or system to meet desired needs.

Outcome 6. Proficiency in the use of computers and other modern tools to solve engineering problems.

Outcome 8. Proficiency in communicating ideas and information orally and in writing.

Prepared by: C. E. Stroud

Date: February 19, 2004