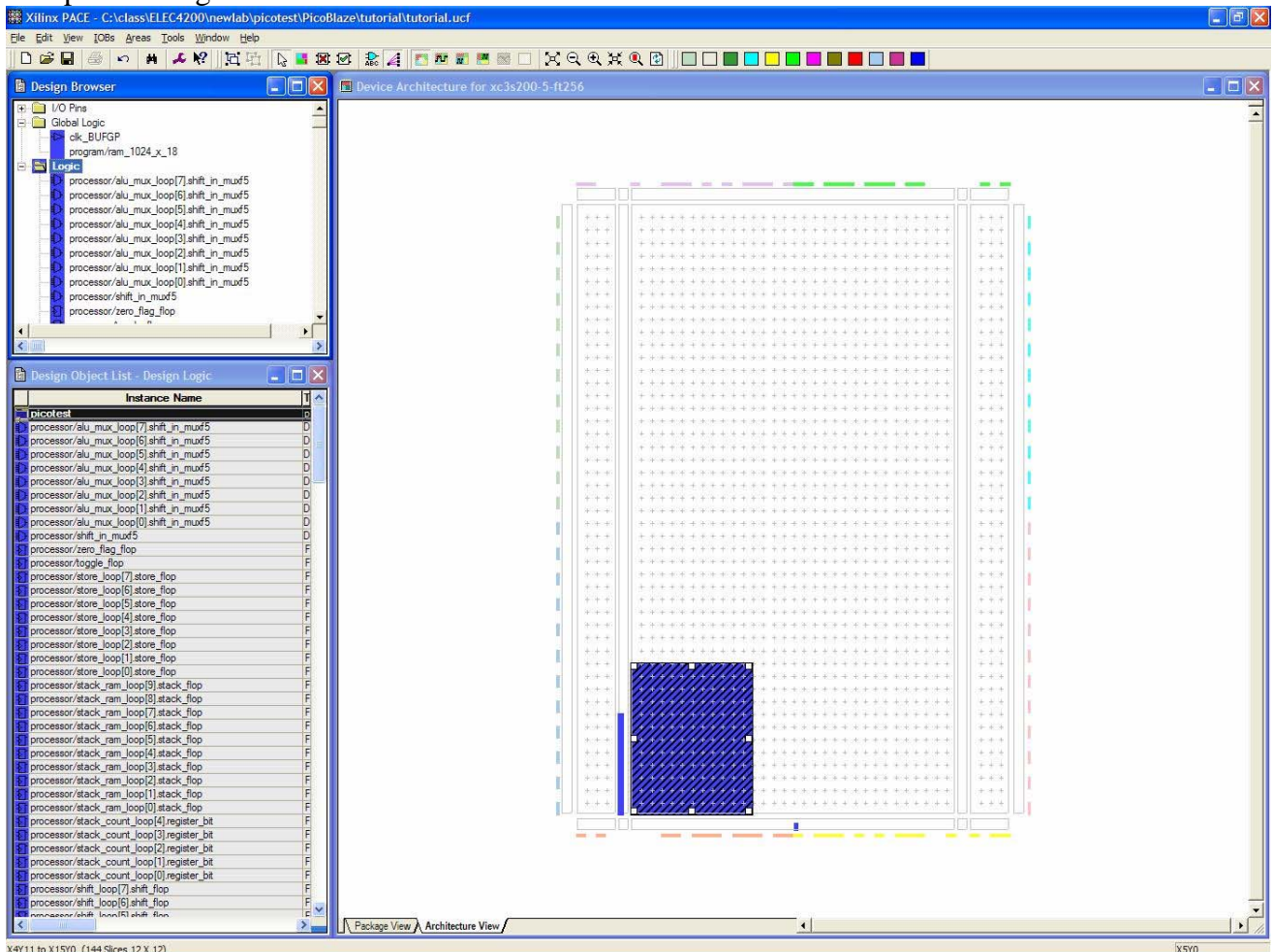
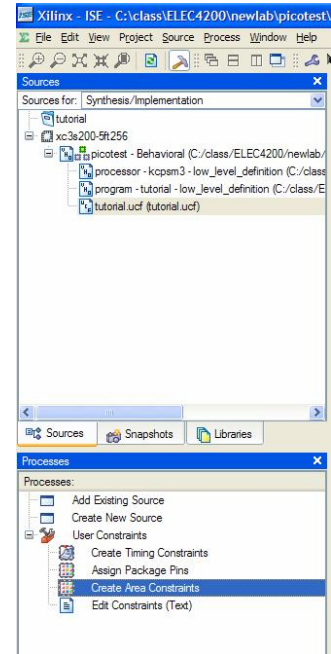


Overview of PACE

PACE is a Pin and Area Constraints Editor which allows you to control the placement of various components in the FPGA during the synthesis process. This helps to facilitate implementation of more customized and optimized circuits within the FPGA. Once a User Constraint File (.ucf) has been added to a project, click on the .ucf file in the **Sources** window, expand the User Constraints in the **Processes** window, and run the Create Area Constraints, as illustrated to the right. This will open PACE as shown below. By expanding the **Design Browser** fields, individual components or groups of components can be selected by clicking the left mouse button and while holding the left mouse button, dragged to the **Device Architecture** window where a box will appear based on the number of slices obtained from the initial synthesis process. The box can be move by clicking and hold the left mouse button while moving the cursor to the desired physical location. The size of the box can be changed by clicking on the small white boxes along the sides and corner, however, it should be noted that the box cannot be made smaller than the area required for the design. Not that in the figure below we have a PicoBlaze core and program memory located next to each other. Once the design has been synthesized, you can go into FPGA Editor and verify that the design was placed within the specified region of the FPGA.



Happy PACEing!!!