ELEC 4200 Digital System Design
Fall 2009 –Lecture: WF 3-3:50pm in BR306
Lab in BR320: M 4-6:50pm

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2004 Catalog Data: ELEC 4200 DIGITAL SYSTEM DESIGN (3) LEC. 2. LAB 3. Pr. ELEC 2210 and ELEC 2220. Hierarchical, modular design of digital systems; computer-aided digital system modeling, simulation, analysis, and synthesis; design implementation with programmable logic devices and field programmable gate arrays.

Textbook: *Digital Systems Design Using VHDL* 2nd Ed., by Chas Roth and Lizy John, Thomson, 2008.

Goals: This course introduces the student to the design of digital logic circuits, both combinational and sequential, and the design of digital systems in a hierarchical, top-down manner. The student is also introduced to the use of computer-aided design tools to develop complex digital circuits and to prototyping designs using programmable logic devices and field-programmable gate arrays.

Course Objectives:
1. Ability to use computer-aided design tools for design of complex digital logic circuits
2. Ability to model, simulate, verify, and synthesize with hardware description languages
3. Ability to design and prototype with programmable logic

Prerequisites by topic:
1. Digital logic design and analysis or switching theory
2. Computer system organization and design

Course Outline:

Wk	Lecture Topic	Ch	Laboratory Project
1	Overview of HDLs and programmable logic		No lab
2	Review of combinational logic circuit design and design verificatoin	**1**	**0**) Introduction to lab hardware and software
3	Review of sequential logic circuit design and system-level timing analysis	**1**	No lab - Martin Luther King holiday
4	VHDL syntax, entities, and architectures	**2**	**1**) Schematic capture, simulation and synthesis of combination logic
5	VHDL concurrent and sequential constructs	**2**	**2**) Schematic capture, simulation and synthesis of sequential logic
6	VHDL modeling guidelines and parameterization	**2**	**3**) VHDL modeling, simulation and synthesis of combinational logic
7	VHDL hierarchical design, **Test #1 10/2**	**4**	**4**) VHDL modeling, simulation and synthesis of sequential logic
8	VHDL data type definitions and test benches	**5**	**5**) VHDL parameterized modeling, simulation and synthesis of a universal register/counter
9	VHDL FSM modeling and simulation	**8**	**6**) VHDL parameterized register file with hierarchical modeling and test bench for design verification
10	Boundary Scan Interface	**10**	**7**) VHDL hierarchical modeling, simulation and synthesis of manually controlled display system
11	PicoBlaze microcontroller architecture, operation and instruction set	**9**	**8**) VHDL hierarchical modeling, simulation and synthesis of Boundary Scan controlled display system
12	Programmable logic arrays, programming technologies and interfaces	**3**	**9**) PicoBlaze programming, simulation & synthesis
13	FPGA architectures and operation	**6**	**10**) VHDL hierarchical modeling, simulation and synthesis of PicoBlaze controlled display system
14	PLD/CPLD architectures **Test #2 11/18**	**3**	
15	Testing and testability	**10**	
16	Introduction to Verilog and semester review		**Lab presentations**
17	**Final Exam: Monday 12/14 4-6:30pm**		

Method of evaluating student performance: There will be two exams and a comprehensive final exam (contributing 20% each to the course grade) in addition to the laboratory projects/exercises (contributing 40% to the course grade). All exams will be closed-book, closed-notes, and closed-neighbor. There will be no unannounced quizzes. Note that each student (or designated lab group) is expected to do his/her (or their) own laboratory project. Discussion of various aspects of the project with fellow students (groups) is acceptable, provided that designs are not copied. All laboratory assignments (pre-lab and lab reports) and projects must be turned in on or before the designated date/time to receive credit.

Class attendance and behavior: Students are expected to attend lectures regularly and on time. In case of absence, the student is responsible for all course business conducted in the lecture class. Lab attendance is mandatory, and unexcused absences will be accounted for in the course grade. There shall be no distractive talking or cell phone usage during lecture and lab classes. In addition, there shall be no web-surfing or emailing during the lab session other than that required by the lab exercise.

Computer usage: VHDL modeling, simulation, and synthesis assignments will require the use of Mentor Graphics and/or Xilinx ISE. Information regarding these CAD tools is available on the ELEC 4200 class web page link at www.eng.auburn.edu/~strouce.

Lab groups: Students may work alone or in groups of two (maximum) for the lab sessions. Lab partners must be established by the first regular lab session (Lab #1) and continue with the same partner throughout the entire semester. Lab partners are expected to contribute equally to the pre-lab and lab exercises as well as in writing the lab report. Students who work alone (without a lab partner) will be given special consideration in terms of grading.

Format for Lab Reports: Lab reports are to be typed with a word processor such at MS Word with figures, tables, and any hand drawings clearly labeled, attached, and introduced/explained at the appropriate point in the typed text portion of the lab report. All lab reports should include:

1. Title and number of lab session.
2. Name(s) of person(s) in lab group.
3. Goal of the lab session – this section should describe the objective of the lab session in terms was what was being designed/implemented and what skills are begin developed.
4. Design process – this section should describe the steps of the process used for the complete design and implementation including both pre-lab and lab exercises.
5. Detailed design – this section should present and describe the details of the design (i.e., K-maps, state diagrams/tables, logic equations, VHDL model). VHDL models should be described in terms of how and what each portion of the VHDL code does.
6. Design verification – this section should provide an explanation of steps performed to verify the design including simulation results and a discussion of thoroughness of the design verification process during simulation. This section should also include a discussion of whether the design implementation worked in the FPGA once simulation based design verification was completed; if the design did not work, described why the design error was not detected during simulation and what modifications to the simulation could be made to detect and correct the design error.
7. Conclusions – this section should describe what you learned form the lab session including what went right and/or wrong, as well as what you would have done differently if you had the chance to do the lab over again.