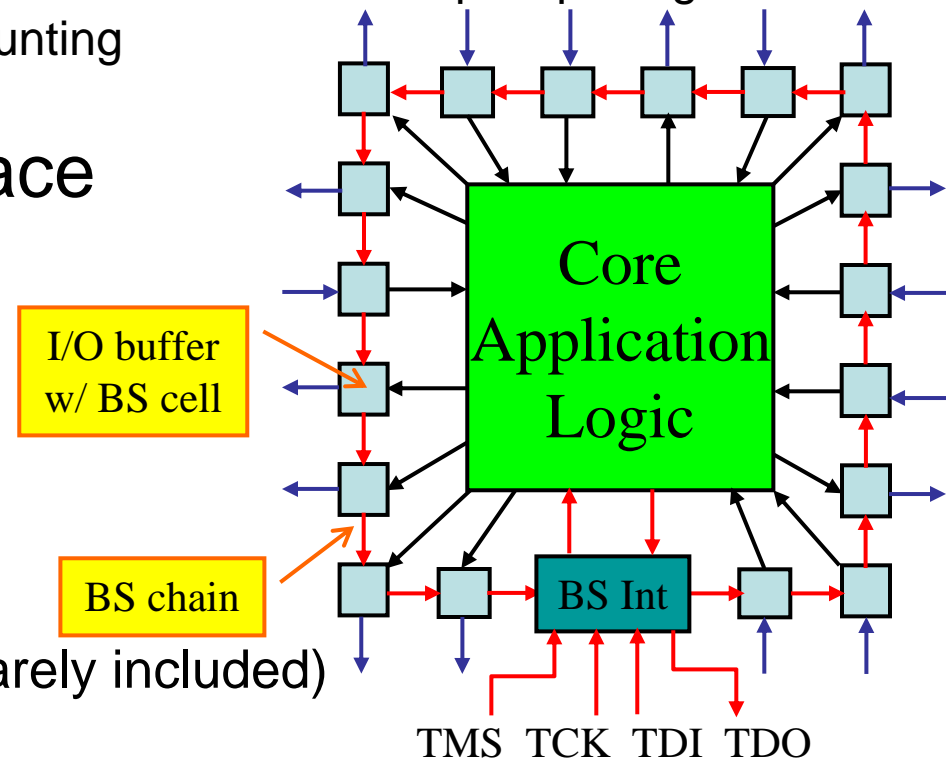


Boundary Scan

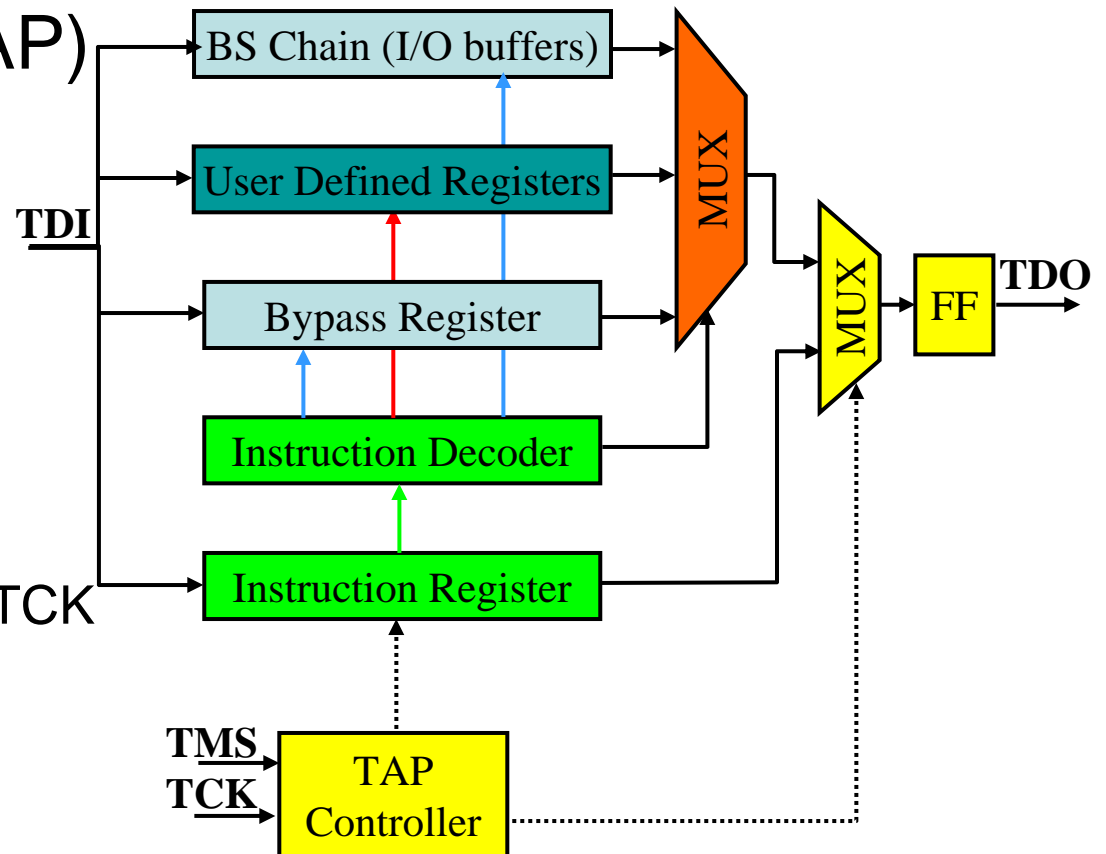
- Developed to test interconnect between chips on PCB
 - Originally referred to as JTAG (Joint Test Action Group)
 - Uses scan design approach to test external interconnect
 - No-contact probe overcomes problem of “in-circuit” test:
 - surface mount components with less than 100 mil pin spacing
 - double-sided component mounting
 - micro- and floating vias
- Standardized test interface
 - IEEE standard 1149.1
 - Four wire interface
 - TMS - Test Mode Select
 - TCK - Test Clock
 - TDI - Test Data In
 - TDO - Test Data Out
 - TRST - reset (optional & rarely included)



Boundary Scan (cont.)

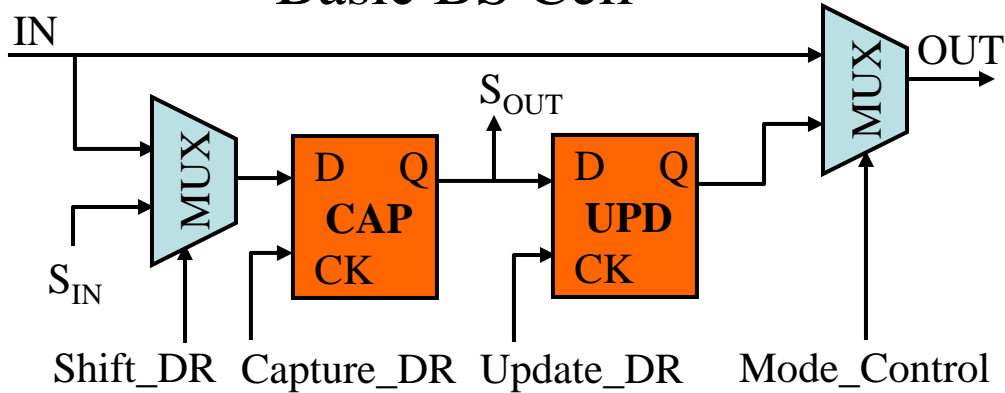
Additional logic :

- 1 Boundary Scan cell per I/O pin
- Test Access Port (TAP)
 - 4-wire interface
 - TMS
 - TCK
 - TDI
 - TDO
 - TAP controller
 - 16-state FSM
 - controlled by TMS & TCK
 - various registers for
 - instructions
 - operations



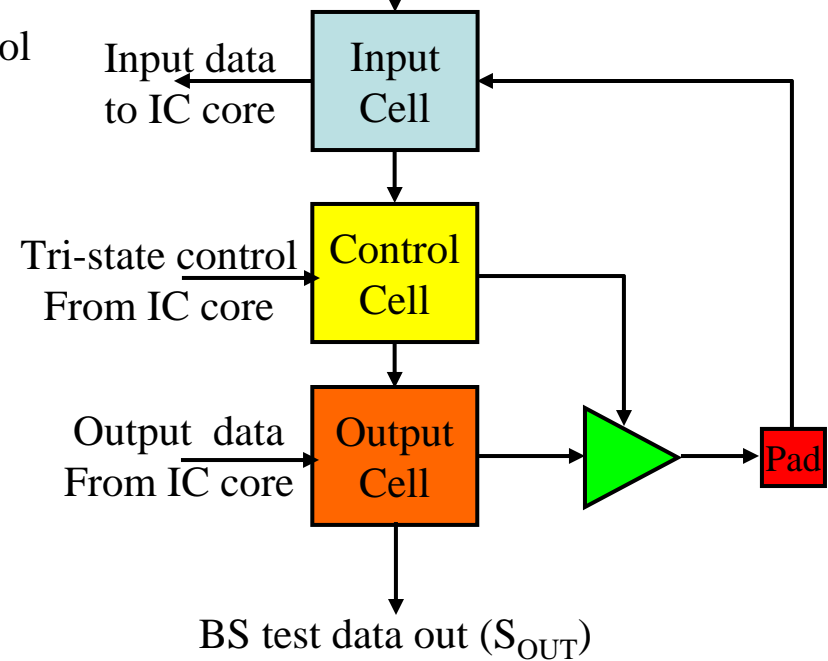
Boundary Scan Cell Architecture

Basic BS Cell



Bi-directional buffers
require multiple BS cells

BS test data in (S_{IN})

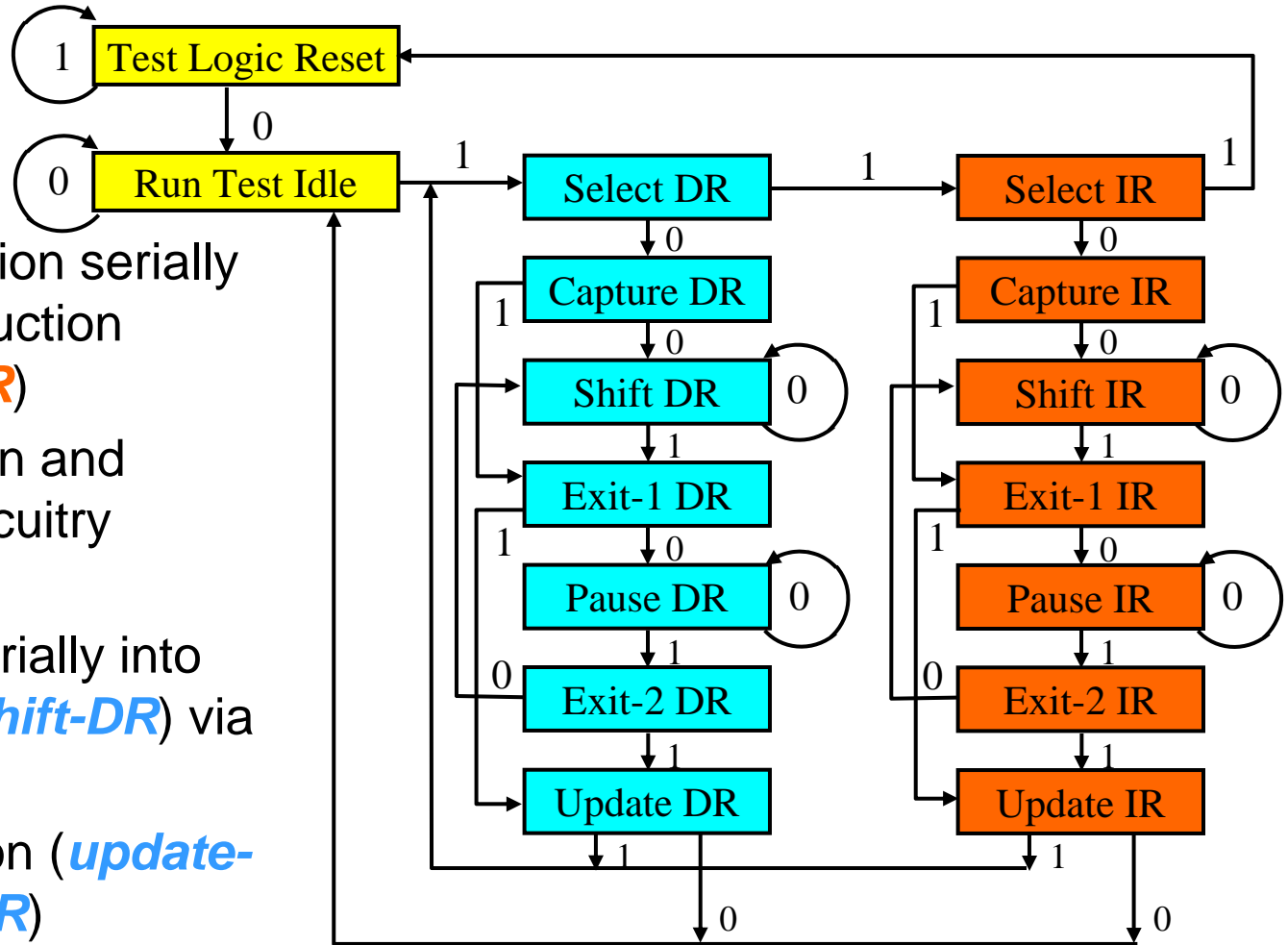


BS Cell Operation

Operational Mode	Data Transfer
Normal Scan	IN \rightarrow OUT
Capture	$S_{IN} \rightarrow$ CAP
Update	IN \rightarrow CAP
	CAP \rightarrow UPD

Boundary Scan TAP Controller Operation

Note: transitions on rising edge of TCK based on TMS value



1. Send test instruction serially via *TDI* into Instruction Register (**shift-IR**)
2. Decode instruction and configure test circuitry (**update-IR**)
3. Send test data serially into Data Register (**shift-DR**) via *TDI*
4. Execute instruction (**update-DR** & **capture-DR**)
5. Retrieve test results captured in Data Register (**shift-DR**) serially via *TDO*

Boundary Scan Instructions

Defined by IEEE 1149.1 standard:

- Mandatory Instructions
 - Extest – to test external interconnect between ICs
 - Bypass – to bypass BS chain in IC
 - Sample/Preload – BS chain samples external I/O
 - IDCode – 32-bit device ID
- Optional Instructions
 - Intest – to test internal logic within the IC
 - RunBIST – to execute internal Built-In Self-Test
 - if applicable (this is rare)
 - UserCode – 32-bit programming data code
 - for programmable logic circuits
 - User Defined Instructions

Boundary Scan: User-Defined Instructions

- User-defined instructions facilitate:
 - public instructions (available for customer use)
 - private instructions (for the manufacturer use only)
 - extending the standard to a universal interface
 - for any system operation feature or function
 - a communication protocol to access new IC test functions
- In FPGAs
 - Access to configuration memory to program device
 - Access to FPGA core programmable logic & routing resources
 - Xilinx is one of few to offer this

Boundary Scan: Advantages

- It's a standard!!! (IEEE 1149.1)
 - allows mixing components from different vendors
 - provides excellent interface to internal circuitry
- Supported by CAD tool vendors, IC & FPGA manufacturers
- Allows testing of board & system interconnect
 - back-plane interconnect test without using PCB functionality
 - very high fault coverage for interconnect
- Useful in diagnosis & FMA
 - provides component-level fault isolation
 - allows real-time sampling of devices on board
 - useful at wafer test (fewer probes needed)
- BS path reconfigured to bypass ICs for faster access

Boundary Scan: Disadvantages

- Overhead:
 - Logic: about 300 gates/chip for TAP + about 15 gates/pin
 - overall overhead typically small (1-3%)
 - but significant for only testing external interconnect
 - especially tri-state (2 cells) & bi-directional buffers (3 cells)
 - I/O Pins: 4
 - 5 if optional TRST (Test Reset) pin is included
 - I/O delay penalty
 - 1 MUX delay on all input & output pins
 - this can be reduced by design
- Internal scan design cannot have multiple chains
- Cannot test at system clock speed
 - But internal BIST can run at system clock speed