Exercise #8

• Design an octal 2s-complement to 8-segment display

• Specifications:
  – The circuit receives 4 inputs (W,X,Y,Z) where
    • W is the sign-bit
    • X-Z is the octal 2s-complement value
      – X is the MSB
  – The circuit produces 8 outputs (A,B,C,D,E,F,G,H) to display the current value where a logic 1 on a given output will turn on its associated display segment
    • Segment H is the sign display (for example, 1010 is -6 and H is on)
    • Note that H is off for either value of +/-0 (0000 & 1000)

• Design the 4-input (W,X,Y,Z), 8-output (A-H) logic circuit:
  a. Generate complete truth table
  b. Generate K-maps
  c. Obtain minimized logic equations
  d. Draw the complete logic diagram for the circuit
Exercise #8 Solution

<table>
<thead>
<tr>
<th>Value</th>
<th>WXYZ</th>
<th>ABCDEFGH</th>
</tr>
</thead>
<tbody>
<tr>
<td>+0</td>
<td>0000</td>
<td>1111100</td>
</tr>
<tr>
<td>+1</td>
<td>0001</td>
<td>01100000</td>
</tr>
<tr>
<td>+2</td>
<td>0010</td>
<td>11011010</td>
</tr>
<tr>
<td>+3</td>
<td>0011</td>
<td>11110010</td>
</tr>
<tr>
<td>+4</td>
<td>0100</td>
<td>01100110</td>
</tr>
<tr>
<td>+5</td>
<td>0101</td>
<td>10110110</td>
</tr>
<tr>
<td>+6</td>
<td>0110</td>
<td>X0111110</td>
</tr>
<tr>
<td>+7</td>
<td>0111</td>
<td>11100X00</td>
</tr>
<tr>
<td>-0</td>
<td>1000</td>
<td>1111100</td>
</tr>
<tr>
<td>-7</td>
<td>1001</td>
<td>11100X01</td>
</tr>
<tr>
<td>-6</td>
<td>1010</td>
<td>X0111111</td>
</tr>
<tr>
<td>-5</td>
<td>1011</td>
<td>10110111</td>
</tr>
<tr>
<td>-4</td>
<td>1100</td>
<td>01100111</td>
</tr>
<tr>
<td>-3</td>
<td>1101</td>
<td>11110011</td>
</tr>
<tr>
<td>-2</td>
<td>1110</td>
<td>11011011</td>
</tr>
<tr>
<td>-1</td>
<td>1111</td>
<td>01100001</td>
</tr>
</tbody>
</table>

A = WX' + YZ' + W'Y + X'Z' + XY'Z
= E + (W'+X)' + W'Y + XY'Z

B = WX + Y'Z' + W'X' + X'Y' + W'YZ
= WX + (Y+Z)' + (W+X)' + (X+Y)' + W'YZ
Exercise #8 Solution

\[ C = WX' + W'X + Z + Y' = F + Z \]

\[ D = X'Z' + YZ' + X'Y + XY'Z = E + (X+Y')' + XY'Z \]

\[ E = YZ' + X'Z' = (Y'+Z)' + (X+Z)' \]

\[ F = Y'Z' + W'X + WX' = (Y+Z)' + W'X + (W'+X)' \]

\[ G = YZ' + XY' + X'Y = (Y'+Z)' + (X+Y') + XY' \]

\[ H = WX + WZ + WY = (W' + X'Y'Z')' = W(X+Y+Z) \]

ELEC 2200

Fall 2012
2-Level AND/OR Minimized SOP Solution

A = WX' + YZ' + W'Y + X'Z' + XY'Z
B = WX + Y'Z' + W'X' + X'Y' + W'YZ
C = WX' + W'X + Z + Y'
D = X'Z' + YZ' + X'Y + XY'Z
E = YZ' + X'Z'
F = Y'Z' + W'X + WX'
G = YZ' + XY' + X'Y
H = WX + WZ + WY

Minimized SOP design with gate sharing gives:
G = 27, Gio = 92, Gdel = 3, Pdel = 21
WCP: a -> p5 -> y' -> y

ELEC 2200  Fall 2012
Optimized for Gio
This circuit: G=24 & Gio=79 😊
worst case timing path analysis:
WCP: a->e->p8->yb->y
Gdel=4 & Pdel=21