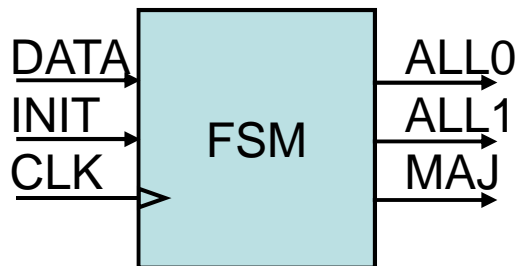


Assignment #9

- Design a rising edge-triggered FSM to report the contents of three consecutive bits and a serial data stream
 - Inputs:
 - DATA – serial data stream to be inspected
 - INIT - active high forces the FSM into a known state depending on the value of the DATA input
 - When DATA=0, next state indicates case where previous 3 bits are 0s
 - When DATA=1, next state indicates case where previous 3 bits are 1s
 - Outputs are don't cares when INIT is active
 - Outputs:
 - ALL0 – active high when 3 consecutive bits are logic 0s
 - ALL1 – active high when 3 consecutive bits are logic 1s
 - MAJ – reports logic value of the majority of the 3 bits being considered



Example sequence: *time*→
INIT = 1010000000000000
DATA = 0011010011000111
ALL0 = X1X0000000001000
ALL1 = X0X1000000000001
MAJ = X0X1110001100011

Assignment #9 (cont.)

- You may choose any combination of D, SR, and JK FFs
- Once you have designed your circuit, write an ASL net list for your circuit and debug/verify the proper operation of your circuit with AUSIM v2.3 (it supports D, SR, and JK FFs)
 - Include your name as a comment in the first line of your ASL
 - Include comment indicating whether your design is Mealy or Moore
 - Input names and ordering: CLK INIT DATA
 - Output names and ordering: ALL0 ALL1 MAJ
- Turn in on paper at beginning of class on the due date:
 - State diagram
 - State table with state assignment
 - Circuit excitation table
 - K-maps
 - Logic equations for combinational logic
 - Complete logic diagram including FFs
 - Copy of your ASL file (.asl file) and simulation results (.out file)
- Email ASL file for working circuit to strouce@auburn.edu before beginning of class on the assignment due date

Assignment #9 (cont.)

- MDA Competition (optional)
 - Choose one (and only one) of the four area & performance metrics for optimization of your circuit
 - G will include gates + FFs as reported in AUSIM v2.3
 - G_{IO} will include gate + FF I/O as reported in AUSIM v2.3
 - G_{del} and P_{del} will be as reported in AUSIM v2.3
 - Include your optimization metric in the first line comment of your ASL file along with your name
 - Email your optimized ASL file for your circuit to strouce@auburn.edu before the beginning of class on the assignment due date