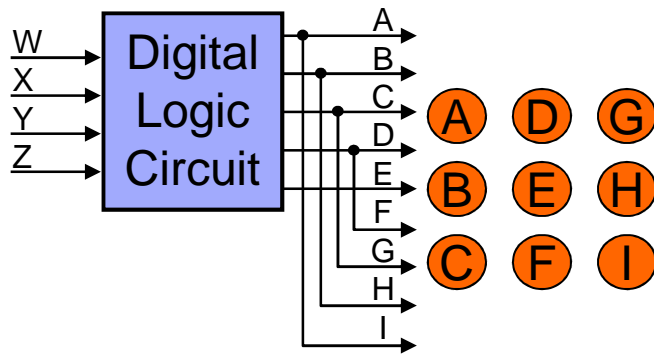


Assignment #6 continue

- Being the hottest digital designer in the history of the world, you immediately observe that the symmetry is such that $A=I$, $B=H$, $C=G$, and $D=F$ which reduces the circuit from 9 outputs to 5 outputs (A-E) as shown below
- You point your observation out to the manufacturer who is so impressed that in addition to your regular pay, the manufacturer offers you a Master Designer Award if, and only if, you can design and verify a working circuit and the circuit is the best working circuit in one of the four following categories from which you may choose one and only one to compete for:
 - Minimum number of gates, G
 - Minimum number of gate I/O, G_{IO}
 - Minimum number of gate delays through the worst case path, G_{del}
 - Minimum propagation delay through the worst case path, P_{del}



Assignment #6 continue

1. Design the 4-input (W,X,Y,Z), 5-output (A,B,C,D,E) logic circuit:
 - a. Generate complete truth table
 - b. Generate K-maps
 - c. Obtain minimized logic equations
 - d. Draw the complete logic diagram for the circuit
2. Verify the design:
 - a. Write an ASL description for your circuit
 - Required input/output names and order: inputs: W X Y Z output: A B C D E
 - Include your name as a comment in the first line of your ASL
 - Read the AUSIM (Ver. L2.2) manual available on the class web page
 - b. Simulate and debug your circuit to obtain a working design
 - Use AUSIM (Ver. L2.2) executable available on the class web page
3. For the Master Designer Award competition, choose one circuit metric (G , G_{IO} , G_{del} , or P_{del}) to optimize your circuit
 - Use Boolean T&Ps or other techniques in your Boolean tool box
 - Use the audits in AUSIM for your analysis of (G , G_{IO} , G_{del} , or P_{del})
 - Simulate and debug your optimized circuit

Assignment #6 continued

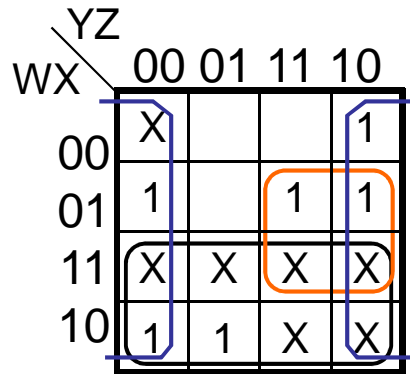
- Steps 1 and 2 are mandatory for this assignment, step 3 is optional (for MDA competition)
- Turn in on paper:
 - Step 1: truth table, Kmaps, logic equations, logic diagram
 - Step 2: print out of your final ASL file and simulation results from AUSIM (.out file)
 - Step 3 (for MDA competition): indicate in the first comment line of your ASL (next to your name) **the** design metric you are competing for (G , G_{IO} , G_{del} , or P_{del}) and the final value you got for that metric (for exmple, $G=13$ for a final gate count of 13)
 - You can only specify **one** metric for MDA competition
- Email your final ASL file to strouce@auburn.edu before the start of class on the day the assignment is due
 - Your ASL circuit must work properly when simulated by the instructor to receive full credit for the assignment **and** to qualify for the MDA competition

Note: a wire from input to output in ASL is not allowed
you must use a 1-input AND or OR gate as a buffer

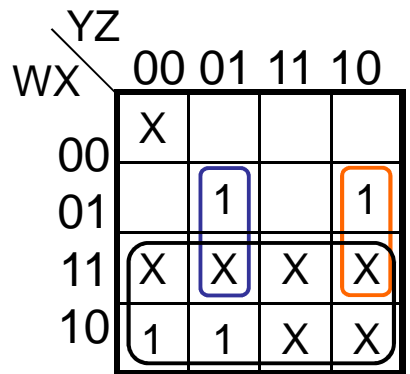
Assignment #6 Solution

1) Truth table

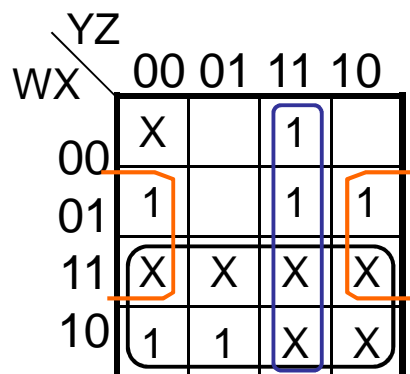
WXYZ	ABCDE
0000	XXXXX
0001	00001
0010	10000
0011	00101
0100	10100
0101	01011
0110	11100
0111	10111
1000	11110
1001	11111
101X	XXXXX
11XX	XXXXX



$$A = W + Z' + XY$$

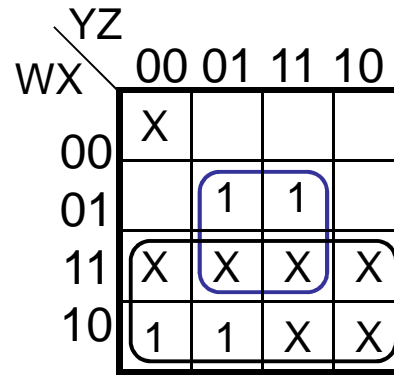


$$B = W + XY'Z + XYZ'$$

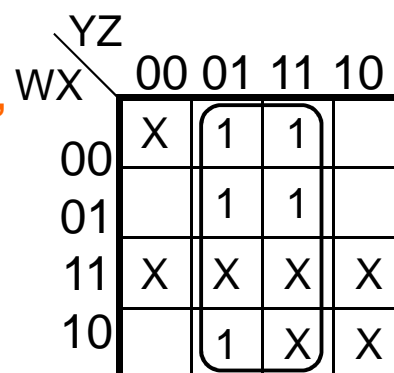


$$C = W + YZ + XZ'$$

2) K-maps & minimized SOPs

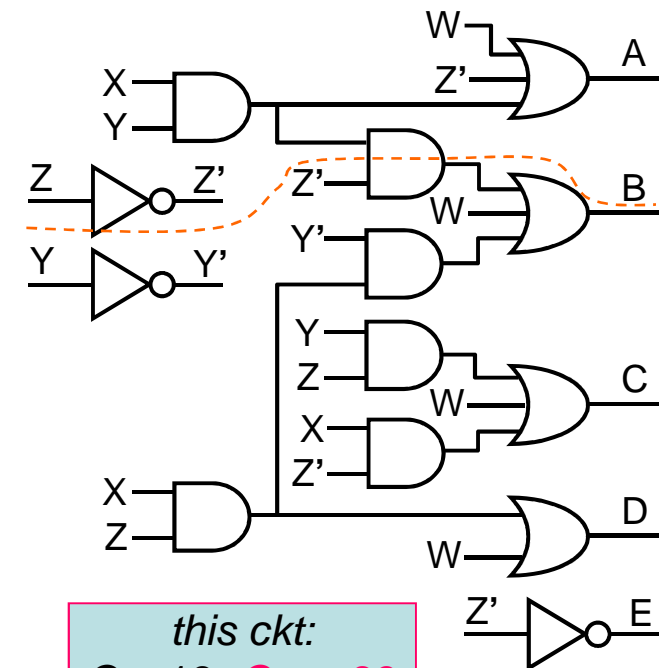


$$D = W + XZ$$



$$E = Z = Z''$$

3) Logic diagram



this ckt:
 $G = 13, G_{IO} = 39$
 $G_{del} = 3, P_{del} = 13$
 wcp: Z \rightarrow Z' \rightarrow B

SOP ckt:
 $G = 13, G_{IO} = 41$
 $G_{del} = 3, P_{del} = 16$
 wcp: Z \rightarrow Z' \rightarrow B

Assignment #6 Solution

```
# ASL for assignment 6 ;
ckt: die in: w x y z
      out: a b c d e ;
not: zn in: z out: zn ;
not: yn in: y out: yn ;
and: a2 in: x y out: a2 ;
or: a in: w zn a2 out: a ;
and: a3 in: a2 zn out: a3 ;
and: a1 in: a6 yn out: a1 ;
or: b in: w a1 a3 out: b ;
and: a4 in: x zn out: a4 ;
and: a5 in: y z out: a5 ;
or: c in: w a5 a4 out: c ;
and: a6 in: x z out: a6 ;
or: d in: w a6 out: d ;
not: e in: zn out: e ;
```

```
# AUSIM (L2.2) Simulation Results ;
# wxyz abcde ;
0001 00001
0010 10000
0011 00101
0100 10100
0101 01011
0110 11100
0111 10111
1000 11110
1001 11111
# no need to simulate 0 & 10-15 ;
# since outputs are don't cares ;
```

MDA Awards for Assignment #6

MDA#1	G=14 (2.5pts each) Bobby Black Bill Tomas	Gio=40 (2.5pts each) Michael Babin Patrick Robinson	Gdel=3 (0.75pt each) Matthew Allsbrook John Capps Daniel Compton Zane Franklin Myers Hawkins Jeff McClellan Jesse Osborne Michael Zekoff	Pdel=13 (3pts) Kent Tomlinson
MDA#2	<i>ties took 1st-2nd</i>	<i>only two entries</i>	<i>ties took 1st-3rd</i>	Pdel=15 (2pts) Joel Lawrence
MDA#3	G=15 (1 pt) JP Creekmore	<i>only two entries</i>	<i>ties took 1st-3rd</i>	Pdel=18 (1pt) Jonathan Boysen
Best in Class	13	39	3	13
Worst in Class	24	89	4	25

Note that 34 of 45 circuits worked and that 17 working circuits did not compete