

Assignment #4 Circuit Analysis

- From this combinational logic circuit, obtain for X and Y:

- Logic Equations
 - directly from schematic
 - then as SOPs
- Truth Table
- Canonical SOPs
- Minterm representations
- Analyze the circuit for:
 - # of gates, G
 - # of gate I/O, G_{IO}
 - # of gate delays, G_{del}
 - Propagation delay, P_{del}
 - ✓ Be sure to specify worst case path for G_{del} & P_{del}

