An Automated BIST Approach for Mixed-Signal Systems

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ABSTRACT: A Built-In Self-Test (BIST) approach that is designed to test the analog portion of mixed-signal systems is described. The majority of the BIST circuitry is located in the digital domain to minimize performance impact on the analog circuitry as well as to facilitate easy and automated synthesis of the BIST circuitry. The BIST approach has been implemented in parameterized VHDL for inclusion in any VHDL-AMS description and supports any size Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) from 4 to 24-bits. The BIST approach provides sixteen test waveforms and three output response analysis modes to test a wide variety of analog application circuits. [1]

1. INTRODUCTION

There are aspects of BIST for analog circuits that prevent the straight forward application of conventional digital test pattern generator (TPG) and output response analyzer (ORA) functions. For example, digital pseudorandom TPGs based on the Linear Feedback Shift Register (LFSR) will produce an analog signal that is similar to noise after passing through a Digital-to-Analog Converter (DAC) [1]. However, ramp input signals have been used in analog testing and have been found to provide good fault detection results and, in some cases, better results than sinusoid test signals [2]. It has been observed that the detection of faults with respect to the input test signal can vary with the type of analog circuit under test [3]. Perhaps a more important consideration is the ORA since traditional digital signature analysis techniques (using LFSRs) are unsuitable for application to analog BIST. In a digital circuit, the good circuit signature is based on the assumption that an exact output response sequence is obtained for every fault-free execution of the BIST sequence [4]. However, in a mixed-signal system, the sampling noise in the DAC and Analog-to-Digital Converter (ADC) as well as processing variations (i.e., tolerances) and environmental variations (i.e., temperature and voltage) in the analog circuitry will prevent an exact output response sequence from one execution of the BIST sequence to the next. As a result, reproducible BIST signatures cannot be obtained for the fault-free circuit.

We have developed a parameterized VHDL description for a BIST approach that tests analog circuitry residing in mixed-signal VLSI devices and systems. The BIST generates sixteen different test waveforms with three modes of output response analysis to test a wide variety of analog circuits. We begin with an overview of the architecture of the mixed-signal based BIST approach in Section 2. In Section 3, we describe the implementation of the BIST approach in parameterized VHDL, the various processor interface options supported in the VHDL model, and the designer's control of the synthesized BIST circuitry provided by the parameterized VHDL generic values. The synthesis results in terms of area and performance measurements are presented in Section 4 for various generic values and processor interface options. The paper is summarized in Section 5.

2. OVERVIEW OF BIST ARCHITECTURE

The BIST architecture is illustrated in Figure 1 with the digital BIST circuitry that has been added to the mixed-signal circuitry shown in bold boxes. The normal mixed-signal system components include the digital and analog system functions as well as the DACs and ADCs that are required to convert the digital signals to analog waveforms and vice versa. The digital BIST circuitry added to the mixed-signal system includes the digital TPG and ORA functions as well as a digital test controller. An additional multiplexer (MUX) is required for the insertion of the digital test patterns into, and isolation of unknown system data from, the data stream at the input of the DAC.

The only BIST circuitry added to the analog domain is the loopback capabilities (analog multiplexers) needed to facilitate the return path for the test signals to the ORA. Since the target circuitry under test is the analog system circuits, including the DACs and ADCs, we incorporate the digital TPG and its associated MUX immediately prior to the digital inputs of the DAC. Similarly, we incorporate the digital ORA at the output of the ADC. This basic architecture has been proposed and implemented in a number of applications [4][5][6] and is referred to as a DAC/ADC loopback BIST [7].

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Figure 1. BIST architecture for mixed-signal systems

The TPG consists of an up/down counter, a Linear Feedback Shift Register (LFSR), and various multiplexers and registers to produce a wide variety of analog test waveforms including ramps, saw-tooth waveforms, triangular waveforms, pseudo-random noise, square wave frequency sweeps with varying and constant amplitudes, as well as DC, step, and pulse test waveforms. In addition, the bit reversal of many of these waveforms is provided where the order of the bits (MSB to LSB) is reversed at the input of the DAC which produces high frequency components in the test waveforms [8].

The ORA is a double precision accumulator that facilitates the determination of a range of values to represent BIST results for the fault-free circuit in order to account for acceptable variations in the output response due to component parameter tolerances, processing variations, voltage/temperature variations, as well as quantization noise in the DAC and ADC. The ORA is capable of summing the analog circuit output response in one of two modes. In one mode, the magnitude of the analog circuit output response is summed in the ORA. In the second mode, the ORA sums the absolute value of the difference between the analog test waveform (output from the TPG) and the analog circuit output response (output from the ADC). This second accumulation mode is useful in detecting faults that cause noise, phase shift, overshoot or ringing in an otherwise good analog circuit response [4][6].

During system-level testing, the test controller ensures proper initialization of the analog circuitry under test, isolation of system data inputs, and length of the test for reproducible results from one execution of the BIST sequence to the next [4]. Faults can be effectively isolated to a given section of analog circuitry by executing the BIST sequences with various configurations of the analog loopback multiplexers illustrated in Figure 1.

3. MIXED-SIGNAL BIST VHDL MODEL

The parameterized VHDL model for the BIST circuitry consists of between 1200 and 1500 non-commented lines of code, depending on the processor interface options chosen by the designer. The model is partitioned into three basic components: TPG, ORA, and test controller. In addition, there are four processor interface options that can be selected by designers for communication with the BIST circuitry in their particular system environment. In the following subsections, we describe those components along with the VHDL generics (summarized in Table 1) used to parameterize the design and provide a variety of system synthesis options to the designer.

Table 1. VHDL Parameterization Generics

Generic	Range	Test Waveform
N_{DAC}	$4 \leq N_{DAC} \leq 24$	# inputs to DAC
N_{ADC}	$4 \leq N_{ADC} \leq 24$	# outputs from ADC
N_{ACUM}	$N_{ACUM} \geq \max(N_{DAC}, N_{ADC})$	# bits in one half of double precision ORA accumulator
N_{PSR}	$N_{PSR} \geq 1$	# Programmable Shift Register bits
N_{ICNT}	$N_{ICNT} + N_{BCNT} \leq N_{ACUM}$	# bits in initialization counter
N_{BCNT}		# bits in BIST sequence counter
N_{LPBK}	$N_{LPBK} \leq N_{ACUM} - 2$	# analog loopback MUX control bits

3.1. Test Pattern Generator

The TPG produces the analog test waveforms but, since the BIST circuitry resides in the digital domain of the mixed-signal circuit, the TPG produces digital patterns that must be passed through a DAC to create a useful analog test waveform. Most DACs on the market today have a resolution ranging from 4-bits to 24-bits.

In order for the VHDL description of the TPG to be a viable addition to an existing mixed-signal design, it must be sized to produce a test pattern that can cover all of these DAC resolutions. A single VHDL generic value specifying the number of bits associated with the DAC, N_{DAC}, is used in the TPG description to size the TPG circuitry to accommodate any desired DAC size from four to twenty-four bits. This value is used to determine the size and functionality of all components within the TPG illustrated in Figure 2 and described in this subsection.

The TPG requires two data registers: a Function Select (FS) Register and a Magnitude Register. The Function Select Register is a 4-bit register whose contents specify the test waveform to be produced by the TPG during the subsequent BIST sequence. The test waveforms and their corresponding binary FS values are given in Table 2. The Magnitude Register is an N_{DAC}-bit register whose contents specify the magnitude that is to be passed to the DAC for the DC, pulse, step, and constant amplitude frequency sweep analog test waveforms. Both registers have an active-high write enable.

Table 2. Function Select Register Definition

FS	Test Waveform	FS	Test Waveform
0	pseudorandom noise	8	DC
1	saw-tooth & ramp-up	9	count-up bit reversal
2	saw-tooth & ramp-down	10	count-down bit reversal
3	triangular wave	11	count-up/down bit reversal
4	frequency sweep w/ varying amplitude	12	freq sweep w/ varying amplitude bit reversal
5	frequency sweep w/ constant amplitude	13	freq sweep w/ constant amplitude bit reversal
6	parabolic ramp	14	parabolic ramp bit reversal
7	pulse	15	step

The Counter/LFSR consists of an N_{DAC}-bit up/down binary counter, that can also perform as an LFSR, and a multiplexer used for bit-reversal of the counter bits. The up/down counter includes an active-high synchronous parallel load and an active-high carry-out. To produce a ramp-up or ramp-down waveform at the output of the DAC, a single pass through an up-count, 0 to N_{DAC}-1, or down-count, N_{DAC}-1 to 0, respectively, would be passed to the DAC. By continuously passing a count-up or count-down to the DAC, a saw-tooth waveform is generated. A triangle waveform can be generated by passing a count-up followed by a count-down to the DAC. To implement the LFSR, the LFSR/Counter must be configured as an LFSR with a primitive

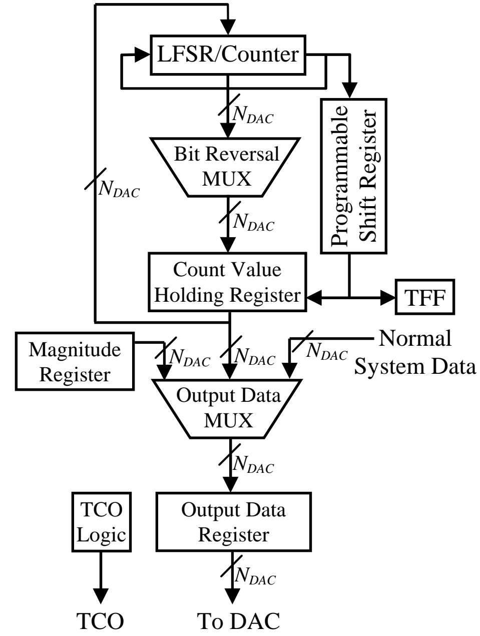

Figure 2. Basic TPG architecture

characteristic polynomial to produce all 2^{NDAC}-1 possible non-zero values. The VHDL description of the TPG automatically determines the appropriate primitive characteristic polynomial based on the generic N_{DAC}, using the polynomials ranging from degrees four to twenty-four given in [4]. The pseudorandom patterns generated by the LFSR appear as white noise once they are passed through the DAC; this type of test waveform is considered to be a universal stimulus and has been used exclusively in a number of mixed-signal BIST applications [1][5][9].

Ramps have also been shown to be effective for fault detection in analog circuits [2][10][11]. The ramp, saw-tooth, and triangular waveforms produced by the counter function of the Counter/LFSR pass directly through the Count Value Holding Register to the DAC. If the Bit Reversal multiplexer is activated, then the ordering of the bits will be reversed; meaning the LSB becomes the MSB and vice versa. This has the effect of producing high frequency components at the output of the DAC for these waveforms. For the frequency sweep waveforms, the Counter/LFSR acts as a binary up-counter, but performs a parallel load of the binary value contained in the Count Value Holding Register each time a carry-out is produced.

The Count Value Holding Register consists of an N_{DAC}-bit parallel-load register. During the frequency sweep waveform generation, the Count Value Holding Register is loaded with the data contents of the Counter/LFSR by the carry-out of Counter/LFSR after being delayed by the Programmable Shift Register. Therefore, for each bit in the Programmable Shift

Register, the carry-out of the Counter/LFSR is delayed by one clock cycle allowing the value in the Counter/LFSR to be incremented before being loaded into the Count Value Holding Register. The contents of this register are then held to be loaded back into the Counter/LFSR on the next active carry-out. The number of bits in the Programmable Shift Register is established by the designer via the generic N_{PSR}, which, in turn, establishes the number of clock cycles that the Counter/LFSR carry-out is delayed before the Count Value Holding Register is loaded, and as a result, the number of times the contents of the Counter/LFSR is incremented before the parallel-load takes place. Therefore, each count sequence of the Counter/LFSR begins at a new starting value with the difference between each starting value being N_{PSR}. For example, if N_{PSR}=1 and N_{DAC}=8, the Counter/LFSR will count 0-255, 1-255, 2-255,…, 253-255, and 254-255. A larger value of N_{PSR} will result in a faster frequency sweep.

The toggle flip-flop (TFF) is enabled to toggle at the same time the Count Value Holding Register is loaded with the contents of the Counter/LFSR and its output is used to enable output data to the DAC (when TFF=1) or to set the output data to the DAC to all zeros (when TFF=0). When the data contents of the Count Value Holding Register are passed to the DAC, a frequency sweep with varying amplitude is produced. Passing the contents of the Magnitude Register to the DAC produces a frequency sweep with constant amplitude. A waveform resembling a parabolic ramp can be generated by forcing the toggle flip-flop to a logic 1 and passing the value of the Count Value Holding Register to the DAC. Like the frequency sweep with varying amplitude, the magnitude of parabolic ramp waveform will continuously increase but will not return to zero.

The Output Data Register is responsible for passing the appropriate data to the DAC for the desired test waveform or operation. The Output Data Register consists of N_{DAC} 3-to-1 multiplexers and logic for selecting output data from the Count Value Holding Register, the Magnitude Register, or the system data input for normal system operation. During frequency sweep test waveforms, the logic in the Output Data Register monitors the TFF output in order to toggle the output from zero to the amplitude stored in either the Count Value Holding Register or Magnitude Register, for a varying or constant amplitude frequency sweeps, respectively.

The Output Data Register also produces the DC, pulse, and step test waveforms. For each of these waveforms, the amplitude stored in the Magnitude Register is passed to the DAC. For the DC test waveform the amplitude is supplied continuously, while it is supplied for only one clock cycle in the case of the pulse or continuously from a given point in time in the case of the step function. The Output Data Register also produces a TPG Carry-Out (TCO) signal for the Test Controller to control the length of initialization and BIST sequences, as will be described in the next subsection. The TCO signal is active-high for a single clock cycle to denote the beginning and end of each test waveform cycle.

3.2. Test Controller

The Test Controller consists of two binary down-counters and a 4-bit control register as illustrated in Figure 3. One of the binary counters (ICNT) controls the length of the initialization sequence while the other counter (BCNT) controls the length of the BIST sequence. The size of the ICNT and BCNT counters, in terms of the number of bits in each counter, are established by the designer using the N_{ICNT} and N_{BCNT} generic values. Prior to testing, both counters function as registers that can be written by the system to establish the desired lengths of the initialization and BIST sequences, respectively. Therefore, the N_{ICNT} and N_{BCNT} generic values establish the maximum length of the initialization and BIST sequences once the BIST circuitry is synthesized while the values written into these registers during system operation establish the actual sequence lengths for a given test sequence. For example, with FS=2 (count-down function in the TPG), a decreasing ramp is produced at the output of the DAC when ICNT=0 and BCNT=1 and FS=2. As another example, consider the input test waveform to and output response from an inverting high-pass filter as illustrated in Figure 4. In this example, if ICNT=0 and BCNT=6, the transient response to the saw-tooth waveform is obtained. On the other hand, if ICNT=6 and BCNT=6, the steady-state response to the saw-tooth waveform may be obtained. Alternatively, if ICNT=0 and BCNT=12, the combination of transient and steady-state responses are obtained.

Once the overall test sequence starts, the ICNT decrements each time TCO is active. When ICNT reaches the count value of 0, it generates a carry-out

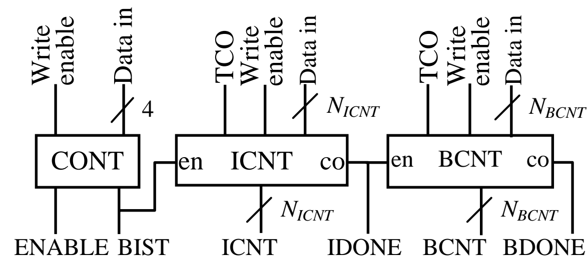

Figure 3. Block diagram of test controller

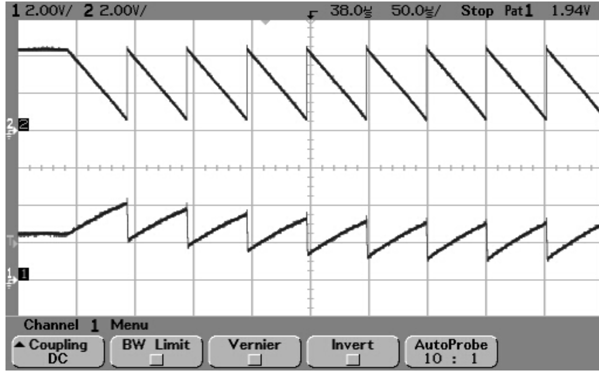

Figure 4. Input test waveform and output response

which sets the Initialization DONE (IDONE) bit in the control register to indicate that the initialization sequence is complete. The active IDONE bit then enables the BCNT to decrement each time TCO is active. When BCNT reaches the count value of 0, it generates a carry-out which sets the BIST DONE (BDONE) bit in the control register to indicate that the BIST sequence is complete. At this time the contents of the ORA can be read to determine the faulty/fault-free status of the analog circuit under test. Output response compaction in the ORA is enabled by an active-high BIST Enable (BEN) signal during the period when IDONE=1 and BDONE=0. As a result, BEN goes inactive at the end of the BIST sequence when IDONE=1 and BDONE=1 which disables the ORA from further data compaction and freezes the resultant BIST signature in the ORA until it can be read by the system for the faulty/fault-free determination.

The remaining two bits in the 4-bit control register include an active-high ENABLE bit that is used to enable the ORA and the test controller along with an active-high BIST bit used to initiate the overall BIST sequence. Only an active ENABLE bit will allow a write operation to the other three bits of the control register to prevent inadvertent generation of BIST waveforms during normal system operation and to minimize power dissipation in the system by preventing data activity in the BIST circuitry.

3.3. Output Response Analyzer

The ORA consists of a multiplexer, an absolute value subtractor, a function register, and the double-precision accumulator as illustrated in Figure 5. One of three output data compaction modes can be selected via the function register and multiplexer. Initially, to test the digital BIST circuitry prior to testing the analog circuitry, the output from the TPG is selected for response compaction in the accumulator via the multiplexer. When testing the analog circuitry, one of two output data compaction modes can be selected: 1) summing the output data from the ADC, or 2) summing the absolute value of the difference between the input test waveform (at the input to the DAC) and the analog output response (at the output of the ADC). Summing the absolute value of the difference in the input test waveform and output response provides the ability to detect faults that results in phase shifts, noise, or ringing/overshoot on an otherwise good output signal [4][6]. The size of the multiplexer and the absolute value subtractor is determined by the N_{DAC} and N_{ADC} generic values.

In addition to providing the select lines for the data multiplexer, the function register also holds loopback control bits (LPBK) for the analog loopback multiplexers located in the analog portion of the mixed-signal system. The number and placement of the analog loopback multiplexers influences the ability to locate and identify faulty analog circuitry. For example, in Figure 1, the loopback at the output of the DAC and input to the ADC allows the DAC and ADC to be tested independently of the rest of the analog circuitry. The number of loopback control bits is specified by the designer via the N_{LPBK} generic value. The function register is controlled by an active-high write enable.

The double precision accumulator consists of two N_{ACUM}–bit registers (ACLO and ACHI). Normally the value of N_{ACUM} is chosen to be the maximum of N_{DAC} and N_{ADC}. However, in cases of small values of N_{DAC} and N_{ADC}, the resulting small accumulator will lead to a lower probability of detecting faults. Therefore, the value of N_{ACUM} can be chosen to be larger than either N_{DAC} or N_{ADC}. Both registers can be written with initial values (typically all 0s) from the processor interface via active-high write enables. The double precision accumulator is enabled to accumulate by the active-high BIST Enable (BEN) produced by the test controller. When BEN goes to 0 at the end of the BIST sequence, the accumulator holds the resultant BIST signature until it can be read via the processor interface to determine the pass/fail status of the analog circuit under test.

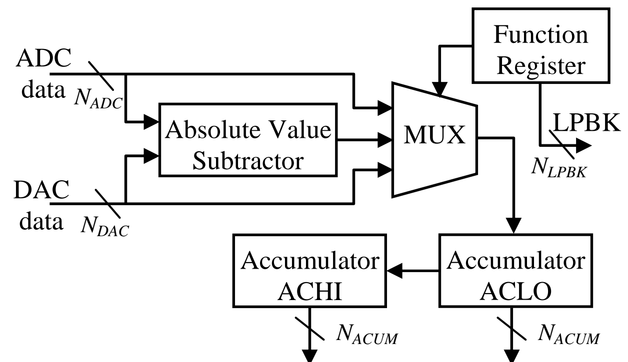

Figure 5. ORA block diagram

The critical timing path in the BIST circuitry lies in the ORA in the path through the absolute value subtractor, data multiplexer, and the double precision accumulator. This limits the maximum clock frequency that can be applied to the BIST circuitry and the resultant frequencies of the test waveforms that can be applied to the analog circuits. However this path can easily be pipelined by inserting flip-flops at the output of the data multiplexer. In addition, a single flip-flop can be added between the carry-out of the ACLO and the count enable of the ACHI for further performance improvements as will be shown in Section 4.

3.4. Processor Interface Options

The Processor Interface is necessary for interfacing to the BIST circuitry in the system in order to initiate and control the various tests and to retrieve the BIST results after each test sequence to determine if the circuit under test is faulty or fault-free. In order to make the BIST circuitry compatible with a variety of system architectures, a number of different processor interface options were developed as illustrated in Figure 6.

The most basic processor interface allows the designer to connect the BIST circuitry to an existing processor interface specific to the mixed-signal integrated circuit or system. This Custom Interface option provides the essential signals needed to read and write the eight data registers of the BIST circuitry. These signals include an active-high write enable, an input data bus, and an output data bus for each register. As a result, the eight individual registers can be grouped in any combination or in combination with other registers in the mixed-signal integrated circuit or system as desired by the designer.

A Parallel Interface option builds upon the Custom Interface option by incorporating an address decoder and a read/write (R/W) signal, to activate the appropriate write enable to one of the eight data registers while using a single input data bus. Therefore, the designer has access only to the 3-bit address, for the eight register addresses, the R/W signal, and the single input data bus. Since the data registers vary in size and the ORA accumulator establishes the size of the largest register, the generic, N_{ACUM}, is used to represent the size of the input data bus. The address decoder produces an active-high write enable for the data register specified by the address signals when the R/W signal is active-high. Similarly, a read multiplexer is incorporated to put the contents of the register selected by the address bits onto a single output data bus (also N_{ACUM}-bits wide). For registers that are smaller than N_{ACUM}-bits, the least significant bits of the data bus are used with logic 0s placed on unused higher order bits.

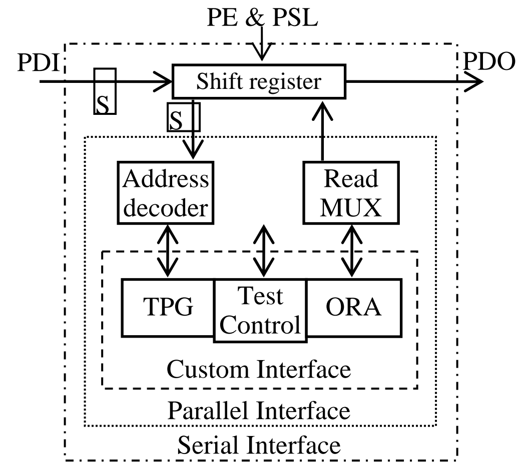

Figure 6. Processor interface options

A Serial Interface option builds upon the Parallel Interface by incorporating an N_{ACUM}+4-bit serial shift register to account for the N_{ACUM}-bit data bus, the 3-bit address bus, and the R/W signal. As a result, the Serial Interface requires only four signals to read and write the eight data registers. These include an active-high Processor Interface Enable (PE), an active-high Processor Interface Shift/Load (PSL), Processor Interface Data-In (PDI), and Processor Interface Data-Out (PDO). Data is shifted into the shift register on PDI when PE=1 and PSL=0. The first N_{ACUM}-bits to be shifted into the shift register correspond to the N_{ACUM} data bits that will be loaded into the selected register, with the LSB being shifted in first. The next 3 bits to be shifted in are the address bits corresponding to the address of the register to be written or read. The last bit to be shifted in is the R/W bit. Once the complete instruction has been shifted in, the operation takes place on the next active edge of the clock when PE=1 and PSL=1. When R/W=1, a write operation occurs, otherwise, the data selected by the output data multiplexer is parallel loaded into the N_{ACUM} bits of the serial shift register. The resultant data read from a register is shifted out when PE=1 and PSL=0.

A final option is the connection of the Serial Interface to the IEEE 1149.1 standard Boundary Scan Interface. To facilitate synchronization between the Boundary Scan Interface and the BIST circuitry, an optional synchronization module can be added at the PE input control to the Serial Interface indicated by the box labeled ‘S’ in Figure 6. This synchronization module is a simple VHDL model consisting of two flip-flops and a digital one-shot. Alternatively, the shift register can be operated directly from the Boundary Scan test clock (TCK) with the synchronization module added at the R/W input of the embedded Parallel Interface as indicted by the second box labeled ‘S’ in Figure 6.

4. SYNTHESIS RESULTS

The parameterized VHDL model for the BIST circuitry using the Serial Processor Interface option was synthesized into 0.5μm CMOS standard cells using Mentor Graphics synthesis for various values of the three primary generics (N_{DAC}, N_{ADC}, and N_{ACUM}). The synthesis results optimized for area are presented in Table 3 and the synthesis results optimized for performance are presented in Table 4.

Table 3. Area optimized VHDL synthesis results

N_{DAC}	N_{ADC}	N_{ACUM}	# Gates	Area (μm^2)	Speed (MHz)
4	4	12	1044	554961	61.3
4	8	12	1100	581594	62.6
4	12	12	1159	624680	64.0
8	4	12	1276	690625	62.6
12	4	12	1506	801766	64.0
12	12	12	1534	809328	64.0
8	8	8	1147	599636	91.8

Table 4. Performance optimized synthesis results

N_{DAC}	N_{ADC}	N_{ACUM}	# Gates	Speed (MHz)
4	4	12	1157	94.0
4	8	12	1227	89.2
4	12	12	1305	86.8
8	4	12	1441	88.9
12	4	12	1716	84.9
12	12	12	1773	85.7
8	8	8	1298	108.7

The maximum clock frequency of the BIST circuitry is dominated by the size of the double precision accumulator as can be seen by the data in the two tables. However, operation in excess of 100 MHz can be obtained for smaller sizes ($N_{ACUM} \leq 9$) that will be more characteristic of many typical applications. In both tables, pipelining flip-flops are included between the output of the data multiplexer and the input of the double precision accumulator. This pipelining produces a speed improvement of over 20 MHz in the synthesized circuit. As can be seen from the tables an additional 20 MHz improvement in speed is obtained with the performance optimization options in the Mentor Graphics synthesis tools. The addition of a single flip-flop between the two stages of the double precision accumulator provides an additional 20 to 25 MHz improvement in the maximum clock frequency (however, this data is not shown in the tables).

We have implemented the BIST circuitry in 1.5 μm CMOS MOSIS TinyChips with one chip containing the TPG circuitry and the other chip containing the ORA and Test Controller. Both chips used the Serial Processor Interface option. We have also synthesized the BIST circuitry into Field Programmable Gate Arrays (FPGAs). We have then used the synthesized BIST circuitry to verify the operation and fault detection capabilities of the BIST approach with benchmark circuits for mixed-signal testing [12][13]. Detection of faults physically inserted in the benchmark circuits has agreed closely with previous fault simulation results of the same benchmark circuits [14].

This VHDL-based BIST approach would also work well in System-on-Chip (SoC) implementations that include embedded an FPGA core and on-board DAC and ADC. The embedded FPGA core in the SoC can be reprogrammed to test the analog portion during off-line testing. Once the analog circuitry has been tested, the FPGA core can be reprogrammed to perform the desired system function. Hence, there are no area or performance penalties associated with the BIST circuitry since it is not incorporated during normal system operation. The only penalty is memory needed to store the BIST configuration for the FPGA core and the download time to reprogram the FPGA core during off-line testing.

5. SUMMARY AND CONCLUSIONS

It has been observed that fault detection in analog and mixed-signal circuits is a function of the different types of test waveforms used for testing [1][2][3][15]. A variety of test waveforms have been used with success on specific analog application circuits including DC, ramps, pseudorandom noise, pulses, and square waveforms of varying frequencies. As a result, a BIST approach with only one type of test waveform is typically effective only for a specific class of circuits. In the search for a generic BIST approach with general applicability to a wide variety of analog application circuits, a number of test waveforms should be provided by the TPG. Similarly, the ORA should provide a number of output response compaction modes in order to increase the probability of detection of faulty behavior such as noise riding on an otherwise good circuit response. For system-level use of BIST, a test controller is needed to provide reproducible results and to facilitate testing transient and/or steady-state responses of the analog circuit under test. While the basic DAC/ADC BIST architecture is not new and has been reported in a number of applications, a test core that can be easily and automatically inserted into any mixed-signal integrated circuit or system is highly desirable [16].

We have presented such a BIST approach for testing the analog portions of mixed-signal systems. The BIST circuitry produces a wide range of test waveforms with multiple output response analysis modes to provide a

high probability of fault detection in a wide variety of analog circuits under test. The test controller provides the ability to test the transient and/or steady-state behavior of an analog circuit under test. The BIST approach has been implemented in a parameterized VHDL model of approximately 1200 to 1500 line of code (not including comments) depending on the processor interface option chosen. This VHDL model facilitates quick and easy incorporation of the BIST circuitry into any VHDL-AMS description and subsequent synthesis of the BIST circuitry with the digital portion of the mixed-signal system. In addition to maximizing the ease with which BIST can be incorporated in the mixed-signal design, placing the majority of the BIST circuitry in the digital domain helps to minimize any adverse performance affects on the analog domain.

The BIST circuitry can be easily customized for any particular application through the specification of the parameterized VHDL generics and the variety of processor interface options without the need for modification or editing of the BIST VHDL code. This eliminates the need for the designer to understand the details of the implementation of the BIST approach. Instead, only an understanding of the overall architecture and operation of the BIST circuitry is required to incorporate and make effective use of the BIST approach in any mixed-signal system application. In addition to the standard cell based digital portion of a mixed-signal Application Specific Integrated Circuit (ASIC), this includes FPGA-based mixed-signal systems and mixed-signal SoC implementations that incorporate embedded FPGA cores. In these programmable logic cases, the BIST circuitry can be configured into the FPGA core only during off-line testing to eliminate any area or performance penalties during normal system operation since the intended system function can be reconfigured into the FPGA core once BIST of the analog circuitry is completed.

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