Analog Circuit Testing Using Built-In Direct-Digital Synthesis

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Abstract: Linearity is an important measure of an analog amplifier performance and normally measured by the 3rd order inter-modulation product (IP3) under a two-tone test. In this paper, we propose a test scheme that generates test tones using a built-in direct-digital synthesizer (DDS). Radio Frequency (RF) test tones are generated by converting the DDS output to RF using a built-in analog mixer that can be the building block of a RF transceiver.

I. Introduction

Analog functional test is a challenging task even for a manual test by an experienced engineer. It tests the functionality of the device against the system specifications. The complexity of the functional test depends on test tasks and the operation frequency. For instance, a base-band amplifier test normally includes its linearity, frequency response, in-band ripple and 3dB cut-off frequency. While for a RF low-noise amplifier (LNA) test, we need to characterize its noise figure (NF), linearity through the 3rd order intercept point (IP3), frequency response including gain, return loss that is related to the input matching.

A few techniques have been suggested to make on-chip frequency-domain testing of mixed-signal circuits. These approaches normally focus on one or two simple parameter tests such as cut-off frequency of a filter and cannot perform rigorous and complete analog tests such as frequency response, linearity, noise and modulation tests. The goal of previous techniques was to overcome the complexity of integrating a traditional AC characterization approach [1]. Well-defined techniques for reducing the size of the test set while maintaining high fault coverage have been reported [2][3]. Some AC test techniques inject optimized digital inputs to a linear device under test and extract a DC signature [4][5]. These approaches are simple, but their precision is limited. On the other hand, Roberts [6-7] has proposed several methods to make frequency-domain tests using on-chip generated sine waves and analyzing the results with an on-chip digital signal processor (DSP). The approach requires 1-bit sigma–delta digital-to-analog converters (DACs) with small area overhead. However, the precision of the generated frequency is not fine enough to support some analog tests such as analog modulation tests using various modulated waveforms and analog linearity tests using precise two-tones.

We propose a direct digital synthesizer (DDS) based testing approach, which can generate various modulated waveform and frequency tones for analog functional test. The DDS approach can provide precise frequency tones for many analog tests such as IP3 measurement and can generate various modulated waveforms such as ramp, step, FSK, PSK, MSK, etc. DDS overcomes the limitations of the traditional phase lock loop analog synthesizer with respect to the cost, resolution, modulation capability, flexibility, stability, and ease of implementation. With the advance of semiconductor technology, the DDS clock frequency can reach as high as a few hundred MHz and most recently has reached even a few GHz. The lookup table is the speed, power consumption and area bottleneck for a traditional DDS architecture. We proposed a delta-sigma noise shaping technique to reduce the number of effective phase bits and thus reduced the size of the look-up table. The DDS die area can be further reduced if the ROM compression technique is utilized [8].

For base-band digital test features such as the test waveform generator, we have designed and synthesized the functionality in a Field Programmable Gate Array (FPGA) and thus verified the concept. The test circuitry, including the DDS, resides in the digital portion of the mixed-signal system to minimize performance impact on the analog circuitry. The proposed test scheme utilizes the existing DAC(s) associated with conventional transceiver base-band architecture. For Radio Frequency (RF) test, the test tones are generated by converting the DDS output to RF using a built-in analog mixer that is also a building block of a RF transceiver. Thus, the proposed analog test scheme provides accurate analog testing means without adding much extra hardware.

II. Linearity Test Using 3rd Order Intercept Point

Intermodulation is a troublesome effect in RF systems, yet is widely used to measure the system linearity. The phenomenon arises when two signals with different frequencies (assume ω_1 and ω_2) are applied to a nonlinear system; the output in general exhibits some components that are not harmonics of the input fundamental frequencies. Of particular interest are the 3rd-order intermodulation (IM) products at $2\omega_1$-ω_2 and $2\omega_2$-ω_1; this is because that if the difference between ω_1 and ω_2 is small, the components at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 appears in the vicinity of ω_1 and ω_2, thus revealing nonlinearity. The corruption of signals due to 3rd-order IM of two nearby interferers is very common and critical so that we use 3rd-order intercept point (IP3) as a figure-of-merit for linearity or distortion. Higher IP3 means better linearity and less distortion. IP3 is commonly tested using two input tones. As an example, the inputs to our experimental amplifier under two tone test are at 498 KHz and 500 KHz, respectively. At the output of the amplifier there are two desired fundamental signals. Because the amplifier is not perfectly linear, it also produces two 3rd-order IM (or IM3) products. IM3 is often given in dBm. The IM3 distortion products are very close in frequency to the desired signals and they cannot be removed easily by filtering. To reduce 3rd-order distortion products, the IP3 specification must be increased.

The 3rd-order IM products are the result of inter-mixing the two-tone inputs by the nonlinearity in the amplifier or mixer. The two IM3 products are:

$f_{IM3\_1} = 2f_1 - f_2$=498x2 - 500= 496KHz;
$f_{IM3\_2} = 2f_2 - f_1$=500x2 - 498 =502KHz.

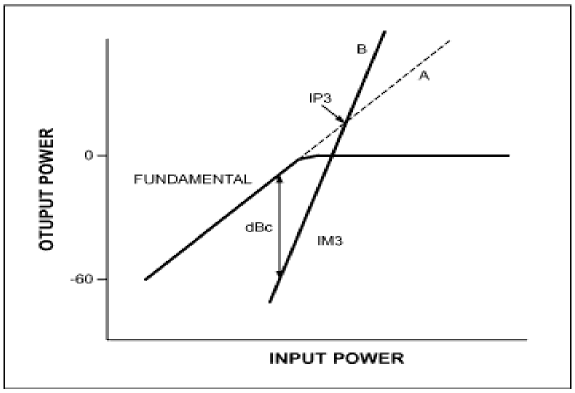


Figure 1. Calculation of 3rd-order Intercept Point.

In mathematical terms, IP3 is a theoretical input power point at which the fundamental and 3rd-order distortion output lines are intercepted as shown in Figure 1. Line A is the output power vs. input power curve for the fundamental (desired) signal, and line B is 3rd-order distortion output power vs. input power curve. The slope for line B is three times as steep (in dB) and theoretically intersects line A. The intercept point is the 3rd-order intercept point. The hypothetical input power at this point is the input IP3 and the output power is the output IP3. The input referred IP3 (IIP3) can thus be found as

$$IIP_3[dBm] = \frac{\Delta P[dB]}{2} + P_{in}[dBm] \qquad (1)$$

where ΔP is the difference between fundamental and IM3 terms and P_{in} is the signal power at the amplifier input.

III. Test Tone Generation Using DDS

DDS is the process of generating deterministic communication carrier reference signals directly in discrete time with the use of digital hardware. A conventional DDS, shown in Figure 2, includes a digital accumulator that generates the phase word based on the input frequency word, Fr.

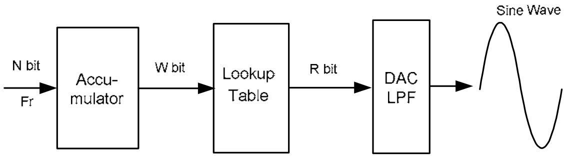


Figure 2. Traditional DDS Structure.

The concept of DDS was described in 1980 by Manssewitz but its implementation was delayed until the 1990s when the IC technology is sufficiently advanced to make it feasible. DDS usually employs the waveform synthesis method. A sine wave, triangular wave, or square wave is computed as a series of samples. These are converted to become an analogue output waveform through a DAC that has to be clocked with a very precise low time jitter clock waveform. Low time jitter is equivalent to having low phase noise. Furthermore because there are no feedback loops in the DDS, the frequency of the output can be made to change instantaneously whenever a new frequency is commanded. With suitable design of the digital circuit that generates the samples values, phase coherence suitable for low spurious fast frequency hopping can also be obtained.

The synthesizer step size is defined as fclk/(2N). Fine resolution can thus be achieved using large accumulator size. The DDS utilizes a sine lookup table to convert the phase word to a sinusoidal amplitude word, whose length is normally limited by the finite number of input bits of the DAC. Deglitch filters are added after the DAC to remove the spurious components generated in the data conversion process. The output frequency is:

$$f_{out} = \frac{F_r f_{clk}}{2^N} \qquad (2)$$

For an IP3 test of an amplifier, the inputs to the device under test (DUT) require two sine waves. For a traditional DDS, we can only generate one sine wave output according to the single frequency increment word Fr. We thus improved traditional DDS with the new structure showed as Figure 3, where the outputs of two DDSs are superimposed using an adder to generate the two-tones used in the IP3 measurement. Note that the two sine lookup tables can be combined to save the die area if the look-up table can operate at the twice of the DDS clock frequency.

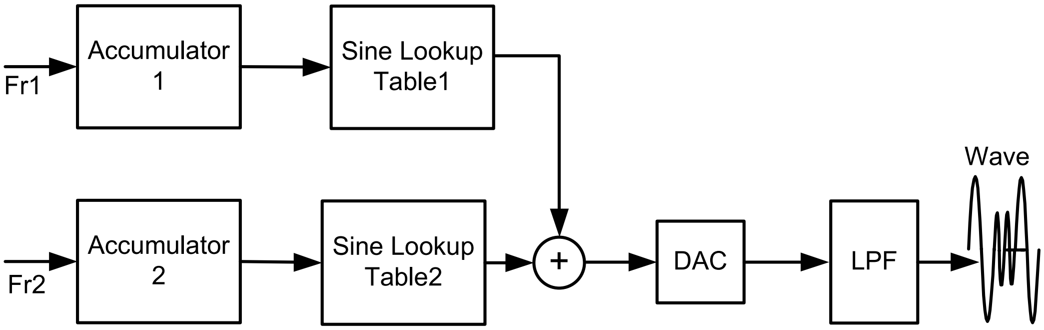


Figure 3. Improved DDS for Two-Tone Generation in an IP3 Test.

IV. Frequency Response Test Using DDS

Frequency response (both amplitude and phase response) is the key measure for integrated low-pass filters (LPFs) and amplifiers. The commonly interested cut-off frequency of the filters and amplifiers can be found out by measuring the passband and stopband amplitude response, while the linearity (group delay) can be determined from the phase response. To test the base-band LPF in the transceiver RFIC, the DDS integrated in the base-band ASIC generates a single frequency tone that loops back from transmitter to receiver through multiplexer’s control.

The DDS generates frequency tones with fine resolution. It can scan the pass and stop bands of the LPF with fine step size and can thus measure the cut-off frequency and pass-band and stop-band ripples of the filter as shown in Figure 4. One of major problems associated with integrated analog filters is the cutoff frequency variation due to temperature, supply voltage and process variations. If the cut-off frequency can be monitored on the fly during transmission idle period (e.g., the preamble period in WLAN applications), its variation can be constantly compensated using built-in tunable circuitry in LPF designs.

With wireless standards operating in very different frequency bands, market leading wireless solutions have to offer multi-mode interoperability with transparent worldwide usage. Thus, the base-band gain stage needs to be tunable for different wireless standard. The proposed test scheme can be used to calibrate the frequency response of the base-band gain stage and LPF in this connection.

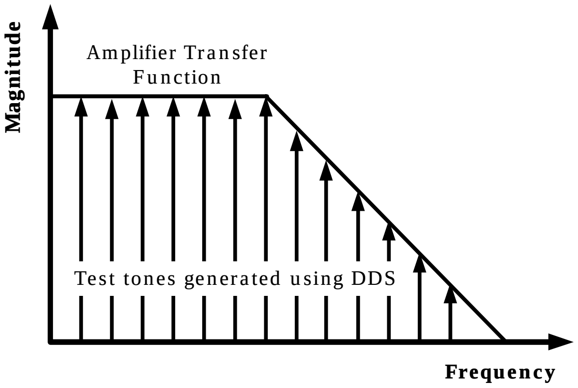


Figure 4. Frequency Response Test Using DDS for Test Tone Generation.

V. Implementation and Measurements

A complete IP3 linearity test configuration using DDS is shown as Figure 5. An analog amplifier is placed after the deglitch LPF as the DUT for IP3 test. To realize the test scheme in hardware, we used the following devices, as illustrated in Figure 5:

1. A Xilinx Spartan-II XSA-50 FPGA board, which has logic density up to 50,000 gates and we only used about 15% of the total area for the entire test scheme.
2. An Analog Device AD9777 (DAC) board, which has 16-bit resolution and we used only 8 bits for the IP3 test. The digital inputs support +2.7 V to +5 V CMOS logic families.
3. An AN221E04 field programmable analog array (FPAA) board, which is used to build the linear amplifier as the device under test.

The accumulator and the sine-lookup table of the DDS system is implemented in the FPGA board using Verilog code. The digital outputs of the DDS are used to drive the AD9777 DAC. For instant response, we can select single-ended mode for the AD9777 DAC board. The combinational waveform can be output from the relative output port S3. The DAC output is used to drive the FPAA board, which serves as the DUT. Using a spectrum analyzer we can measure the signal power at the amplifier input and output for IP3 calculation.

To verify concept of the proposed the IP3 test scheme, we compare the measured waveforms and spectra to the simulated results. The output of the DAC is a composed waveform, which include two sinusoidal waves, as shown in Figure 6 and Figure 7 for both simulated and measured waveforms and spectra. The DDS is implemented in a FPGA as described above. The simulation was done using both MATLAB and Verilog HDL. The MATLAB and Verilog simulation results are compared to each other to achieve bitwise matches between MATLAB behavioral and Verilog HDL simulations. The two sine waves with different frequencies are generated according to its frequency increment words Fr1 & Fr2. Figure 6 and Figure 7 demonstrate good agreement between the simulated and measured DDS outputs.

The AN221E04 device consists of a 2x2 matrix of fully configurable analog blocks (CABs). The FPAA configuration data is stored in an on-chip SRAM configuration memory.

Figure 8 presents the output spectrum of the amplifier with two-tone inputs generated using DDS. Again, the simulated amplifier spectrum using MATLAB is compared to the measured spectrum obtained from an Agilent spectrum analyzer in a test configuration as shown in Figure 5. Figure 8 clearly demonstrates the expected IM3 terms close to the desired fundamentals. Using Eq. (1), we can thus measure the IP3, namely, the linearity of the DUT amplifier with the automatically generated two-tones using built-in DDS.

As a test example, an amplifier operates around 500 KHz is programmed in the FPAA. The amplitude of the two-tone test signal from DDS output is -15.17dB (Figure 7b) and the two test tones are at the frequencies of 498 KHz and 500 KHz.

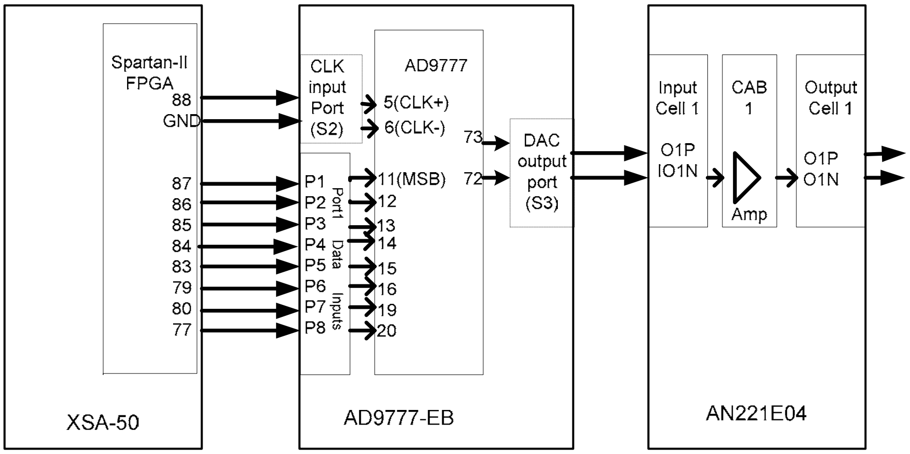
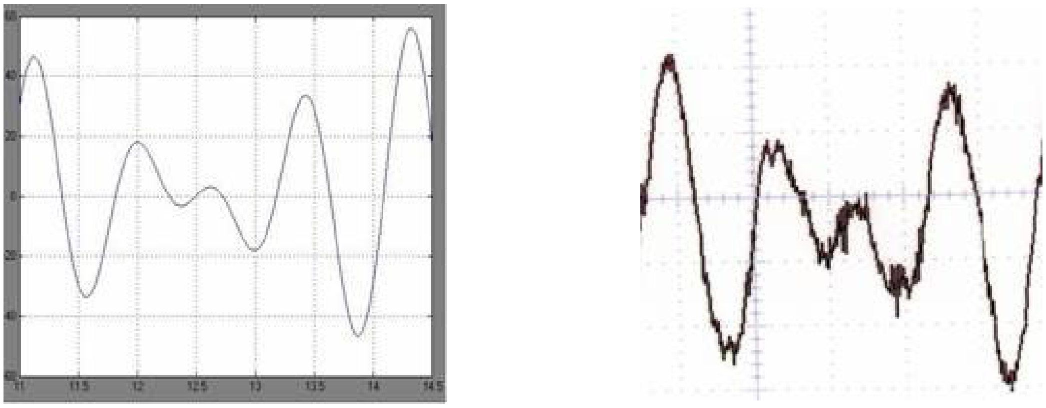
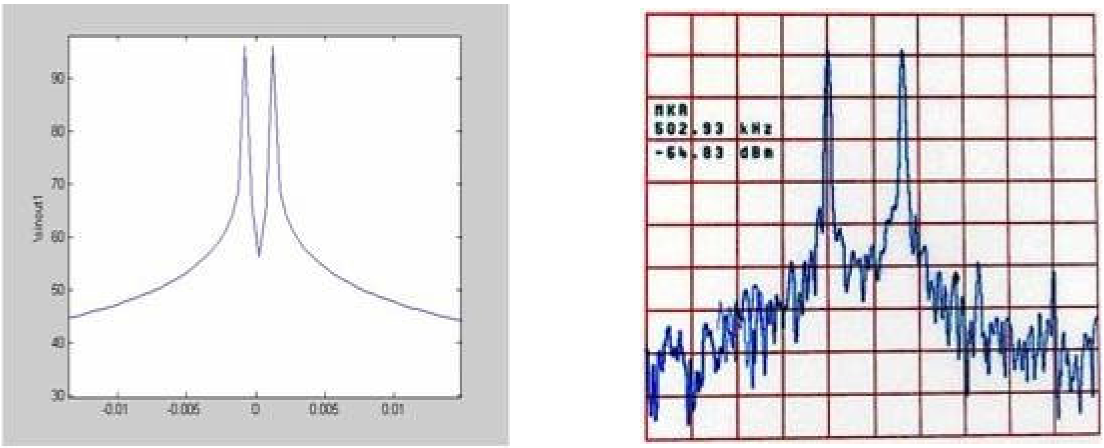


Figure 5. Linearity Test Configuration.



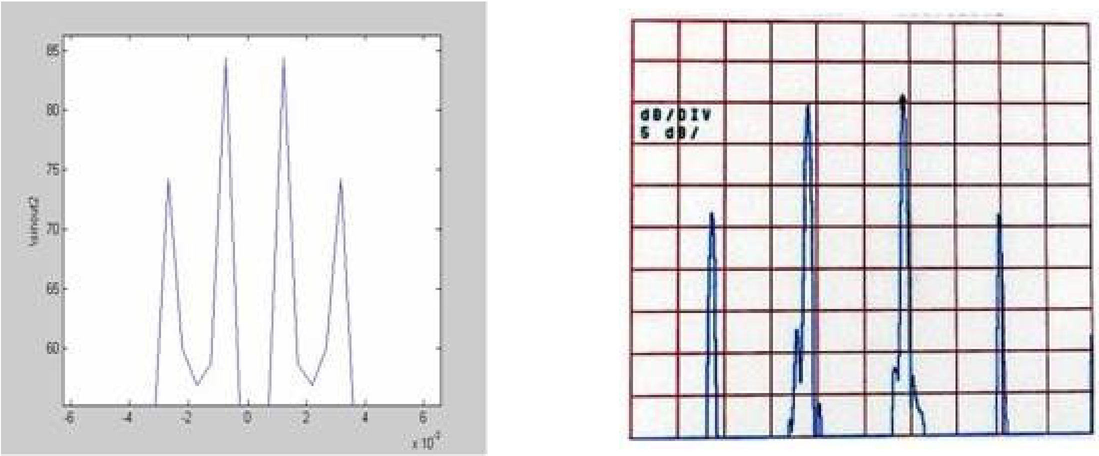
(a) Simulated output waveform.
(b) Measured output waveform using digital scope.

Figure 6. DDS Output Waveform Used for Two-Tone IP3 Test.



(a) Simulated output spectrum.
(b) Measured output spectrum using spectrum analyzer.

Figure 7. DDS Output Spectrum of the Two Tones Used for IP3 Test.



(a) Simulated output spectrum.
(b) Measured output spectrum using spectrum analyzer.

Figure 8. Amplifier (DUT) Output Spectrum with Two-Tones Generated Using DDS.

From Figure 8b, we measured 4 output tones at 496, 498, 500, 502 KHz with magnitude at -24dB, -9.6dB, -9.6dB and -24dB, respectively. Thus, we can determine the input referred IP3 value according to equation (1) as IIP3 = (-9.6-(-24))/2+(-15.17) = -9.97 dBm.

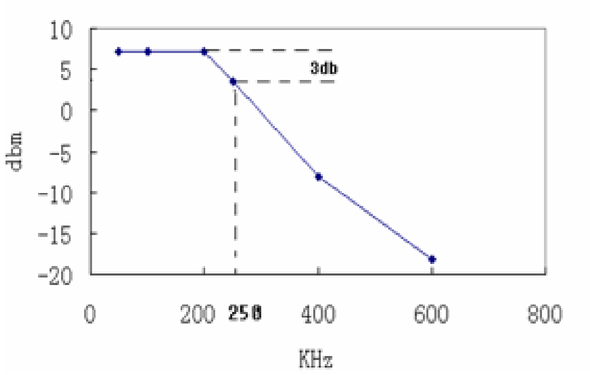


Figure 9. Measured frequency response of an amplifier module using DDS.

We also use the proposed test scheme to measure the frequency response of an amplifier (DUT). As discussed in section IV, the built-in DDS generates the test tones that scan over the pass and stop bands (from 50 KHz to 600 KHz) of the DUT. An amplifier and a low pass filter are programmed in FPAA with the 3dB cut-off frequency to be measured. We apply the test tones at the input of the filter and measure its output magnitude response using either a digital scope or a spectrum analyzer. The measured amplifier output response is shown in Figure 9. The cutoff frequency of the amplifier and LPF modules, which is 3dB below the pass-band magnitude, can thus be found out as 250 kHz from Figure 9. The proposed test scheme can also be used to measure the pass-band and stop-band ripples and the roll-off slope of the filter. The proposed measurement is also useful for cut-off frequency monitoring, which is important to calibrate and compensate the cut-off frequency variations due to process, temperature and supply voltage variations.

VI Conclusions

We have proposed a built-in automatic test scheme for testing the linearity of analog modules using a built-in DDS. The concept has been proved both in simulations and in hardware implemented using a FPGA for test signal generator and a FPAA for DUT (amplifier module). The simulated and measured data show good agreement in linearity (IP3) measurement. In addition, the implementation in an FPGA illustrates one potential system-level use of the approach where an existing FPGA in the mixed-signal system that interfaces to the DAC is reconfigured during off-line testing to implement the DDS circuitry for in-system testing and measurement of analog functionality. Once testing is complete, the FPGA can be reconfigured with the original system function, avoiding any area overhead or performance penalty associated with the DDS circuitry. Future work of the linearity test scheme will include both the built-in test generator and test response analyzer to form a complete automatic analog built-in self-test flow.

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