



Phase Delay Measurement and Calibration in Built-In Analog Functional Testing

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Abstract—A Built-In Self-Test (BIST) approach has been proposed for functionality measurements of analog circuitry in mixed-signal systems. The BIST circuitry consists of a direct digital synthesizer (DDS) based test pattern generator (TPG) and multiplier/accumulator (MAC) based output response analyzer (ORA). In this paper we investigate and discuss the effects of phase delay on analog functionality measurements in mixed-signal systems when using MAC-based ORAs. We show that phase delay has a critical impact on measurement results and that the MAC-based ORA is an effective method for measuring phase delay.

I. INTRODUCTION AND BACKGROUND

Mixed-signal Built-In Self-Test (BIST) is now in more demand than ever. First, analog functionality tests based on the traditional methodology of manual testing costs much more money and time due to the ever-increasing operational frequency and complexity of modern mixed-signal integrated circuits (ICs). For example, radio frequency integrated circuit (RFIC) test cost can be as high as 50% of the total cost, depending on the complexity of the functionality to be tested [1]. Second, the operational frequency and complexity of modern mixed-signal ICs make it difficult to perform test on these ICs. Finally, with a rapidly increasing level of integration, the number of input/output (IO) pins does not increase accordingly such that observability of internal components is lower compared with traditional ICs [2]. Therefore, it becomes more attractive to automate the analog testing process with low-cost, built-in test circuitry.

In order to perform a suite of analog functionality tests, such as linearity, frequency response, and noise figure (NF) measurement, in a BIST environment, the frequency spectrum of the signal coming from the device under test (DUT) needs to be measured and analyzed by an output response analyzer (ORA) included in the BIST circuitry [3]. A few techniques have been proposed to perform on-chip frequency-domain testing of mixed-signal circuits in [4]–[7]. However, most of these approaches focus only on one or two simple parameter tests such as cut-off frequency of a filter

and cannot perform complete analog tests such as frequency response, linearity, and noise measurements [1].

A new mixed-signal BIST approach has been proposed which includes a direct digital synthesizer (DDS) based test pattern generator (TPG) and multiplier/accumulator (MAC) based output response analyzer (ORA). Because the signal is in digital form, it is easy to include different modulation capabilities in the DDS. Therefore, many analog functional tests, such as magnitude and phase response in the frequency domain, 3rd order intercept point (IP3) and noise figure (NF) can be performed in this architecture [1]. Some experimental results for IP3 and frequency response (both phase and gain) using this BIST architecture have been presented in [1] to demonstrate the feasibility and accuracy of the BIST approach.

In this paper, we discuss the effect of phase delay on the implementation and accuracy of the MAC-based ORA. In addition, through experimentation with the BIST circuitry, a simple comparison between the MAC-based ORA and FFT-based BIST scheme is also presented. The paper is organized as follows. Section 2 gives an overview of the BIST approach. This is followed by a detailed discussion of the effect of phase delay on the MAC-based ORA in Section 3. Some experimental results related to the MAC-based ORA are presented in Section 4 and the paper concludes in Section 5.

II. OVERVIEW OF BIST ARCHITECTURE

The mixed-signal BIST architecture, illustrated in Fig. 1, is capable of accurate on-chip analog functional measurements [1]. In order to minimize the area and performance penalty on the analog circuitry, the majority of the BIST circuitry resides in the digital portion of the mixed-signal system. The digital portion of the BIST circuitry includes a DDS-based TPG, a MAC-based ORA, and a test controller. The test scheme utilizes the existing digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) typically associated with most mixed-signal architectures to provide accurate analog functionality testing and measurements while minimizing the hardware added for BIST. The only test circuitry added to the analog domain is loopback capabilities needed to facilitate one or more return paths for the test signals to the ORA. The number and location of these loopback capabilities determines the accuracy and resolution of tests and measurements associated with a given analog function.

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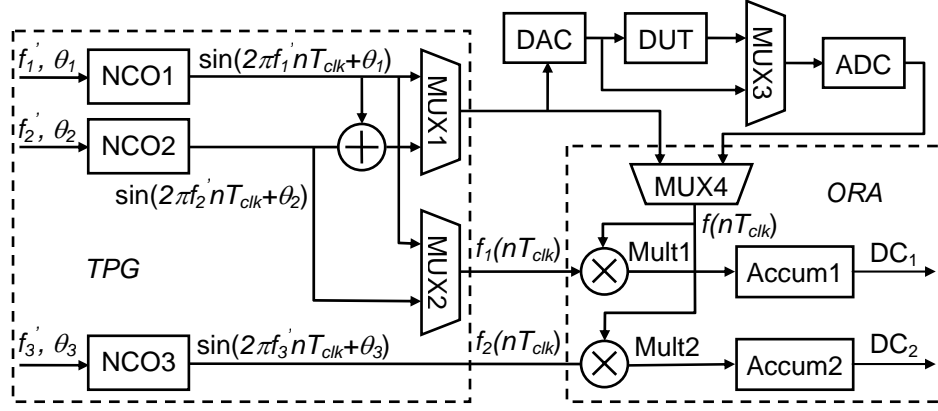


Fig. 1. General model of BIST architecture.

The DDS-based TPG consists of three numerically controlled oscillators (NCOs) and utilizes the existing DAC from the mixed-signal system to complete the DDS. Fig. 2 shows a more detailed view of the numerically controlled oscillator (NCO) used in the TPG. The phase accumulator is used to generate the phase word based on the frequency word f and the initial phase word θ . Then the NCO utilizes a look-up table (LUT) to convert the truncated phase word sequence to a digital sine wave sequence shown in Fig. 2. The output sine wave frequency is determined as

$$f' = \frac{f \cdot f_{clk}}{2^n}, \quad (1)$$

where n is the word width of the phase accumulator. The digital sine wave serves two purposes. One purpose is to produce an analog stimulus to the DUT through the DAC. The other is to provide in-phase and out-of-phase test tones for the MAC-based ORA.

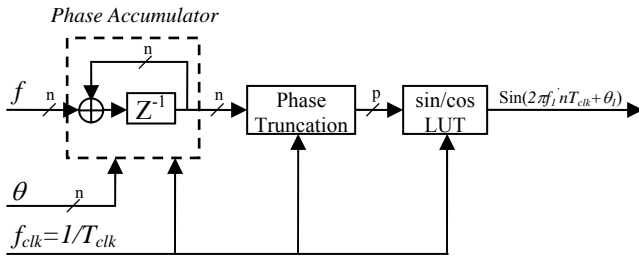


Fig. 2. NCO used in TPG.

The ORA consists of two sets of $N \times N$ -bit multiplier and M -bit accumulator pairs with each MAC performing in-phase and out-of-phase analysis respectively. In the design of the ORA, N is the number of bits from the DDS and ADC and M is chosen such that $K < 2^{M-2N}$, where K is the length of the BIST sequence in clock cycles. A more detailed description of how the MAC-based ORA works is given in the following section.

III. OVERVIEW OF PHASE DELAY

While performing the frequency response, linearity and NF measurements, $f_1(nT_{clk})$ and $f_2(nT_{clk})$ is set to $\cos(\omega nT_{clk})$ and $\sin(\omega nT_{clk})$ respectively. As a result, the DC_1 and DC_2 accumulator values can be described as

$$DC_1 = \sum_n f(nT_{clk}) \cdot \cos(\omega nT_{clk}), \quad (2)$$

$$DC_2 = \sum_n f(nT_{clk}) \cdot \sin(\omega nT_{clk}). \quad (3)$$

From (2) and (3), it can be seen that DC_1 and DC_2 are the in-phase and out-of-phase components of the signal $f(nT_{clk})$ at frequency ω . The signal $f(nT_{clk})$'s Fourier Transform $F(\omega)$ can also be expressed through DC_1 and DC_2 according to the following formula:

$$F(\omega) = \sum_n f(nT_{clk}) \cdot e^{j\omega nT_{clk}} = DC_1(\omega) + j \cdot DC_2(\omega) \quad (4)$$

From (4), the signal $f_1(nT_{clk})$'s frequency spectrum, $F(\omega)$, within the bandwidth can be measured through the DC_1 and DC_2 by sweeping the frequency ω over the interested bandwidth. In comparison with the FFT which computes $F(\omega)$ over the entire band at the same time, the MAC-based ORA in Figure 1 only measures $F(\omega)$ at one frequency point at a time with the entire spectrum obtained through successive measurements.

From the function $F(\omega)$, the amplitude $A(\omega)$ and the phase $\Delta\phi(\omega)$ of the spectrum can be derived as follows:

$$F(\omega) = DC_1(\omega) + j \cdot DC_2(\omega) = A(\omega)e^{j\Delta\phi(\omega)}, \quad (5)$$

where

$$\Delta\phi(\omega) = \text{tg}^{-1} \frac{DC_2(\omega)}{DC_1(\omega)}, \quad (6)$$

$$\begin{aligned} A(\omega) &= F(\omega)e^{-j\Delta\phi(\omega)} \\ &= \sum_n f(nT_{clk}) \cdot e^{j[\omega nT_{clk} - \Delta\phi(\omega)]} \\ &= \sum_n f(nT_{clk}) \cdot \cos(\omega nT_{clk} - \Delta\phi(\omega)) \end{aligned} \quad (7)$$

These two parameters are used much more widely in analog functional measurements. The amplitude response $A(\omega)$ is of interest because many important parameters, such as cut-off frequency, in-band ripple, bandwidth, etc., are determined by it. The phase response $\Delta\phi(\omega)$ represents the delay introduced by electrical devices. It is also because of the phase delay that there is normally a phase difference between the external path through the DUT and the internal

path from the TPG to the ORA (refer to Fig. 1).

The phase delay is an important issue to the MAC-based ORA because it will affect the accuracy and implementation of the BIST approach. Once the phase retardation $\Delta\phi(\omega)$ is determined based on (6), $A(\omega)$ can be measured through DC_1 according to (7) if the test tone generated by NCO can be phase-adjusted using $\Delta\phi(\omega)$. However, with pre-determined $\Delta\phi(\omega)$, $A(\omega)$ can also be calculated as follows:

$$A(\omega) = \frac{DC_1}{\cos \Delta\phi(\omega)} = \frac{DC_2}{\sin \Delta\phi(\omega)} \quad (8)$$

For an on-chip test, we don't have to set up a full-length *arctan* LUT to get the exact phase delay from DC_1 and DC_2 . First the quadrant of $\Delta\phi(\omega)$ can be determined from the sign bits of DC_1 and DC_2 . Before we further the discussion, we define a new term, the *absolute phase offset* of $\Delta\phi(\omega)$ in the corresponding quadrant and it can be calculated through the formula as

$$\Delta\phi_o(\omega) = \begin{cases} \text{tg}^{-1} \frac{|DC_2(\omega)|}{|DC_1(\omega)|} & |DC_1(\omega)| \geq |DC_2(\omega)| \\ \text{tg}^{-1} \frac{|DC_1(\omega)|}{|DC_2(\omega)|} & |DC_1(\omega)| < |DC_2(\omega)| \end{cases} \quad (9)$$

The relationship between $\Delta\phi(\omega)$ and $\Delta\phi_o(\omega)$ is shown in Table I. Therefore, $\Delta\phi(\omega)$ can be identified with $\Delta\phi_o(\omega)$ whose value range is $[0^\circ, 45^\circ]$. Upon the analysis until now, the *arctan* LUT can be decreased by half. Furthermore, the *arctan*(DC_2/DC_1) can be represented by the ratio of the DC_2/DC_1 when DC_2/DC_1 is very small. So the length of the *arctan* LUT can be compressed further such that the hardware resources used by the phase calculation can be minimized.

TABLE I
RELATIONSHIP BETWEEN $\Delta\phi(\omega)$ AND $\Delta\phi_o(\omega)$

	$ DC_1 \geq DC_2 $	$ DC_1 < DC_2 $
$DC_1 > 0; DC_2 > 0$	$\Delta\phi(\omega) = \Delta\phi_o(\omega)$	$\Delta\phi(\omega) = 90^\circ - \Delta\phi_o(\omega)$
$DC_1 > 0; DC_2 < 0$	$\Delta\phi(\omega) = 360^\circ - \Delta\phi_o(\omega)$	$\Delta\phi(\omega) = 270^\circ + \Delta\phi_o(\omega)$
$DC_1 < 0; DC_2 > 0$	$\Delta\phi(\omega) = 180^\circ - \Delta\phi_o(\omega)$	$\Delta\phi(\omega) = 90^\circ + \Delta\phi_o(\omega)$
$DC_1 < 0; DC_2 < 0$	$\Delta\phi(\omega) = 180^\circ + \Delta\phi_o(\omega)$	$\Delta\phi(\omega) = 270^\circ - \Delta\phi_o(\omega)$

Basically, there are three techniques to measure and calibrate the phase delay. One is to adjust the phase of the outgoing test tone in the NCO such that the DUT output is in phase with the signal to be mixed in the ORA and then make the amplitude measurement. The second approach is to calculate the corrected amplitude according to (8). The last method is to obtain the amplitude directly from DC_1 and DC_2 as follows:

$$A(\omega) = \sqrt{DC_1^2 + DC_2^2} \quad (10)$$

All these three approaches have their own advantages

and disadvantages. The most attractive merit of first approach is that it doesn't require any extra circuitry to calculate the amplitude once the phase delay is determined. However, there are also some disadvantages associated with it. First, an extra accumulation sequence is required to obtain the amplitude response, which will slow down the processing speed and lengthen testing time. Second, this approach cannot be used for MF measurement. Usually the noise in electric devices is modeled as a white Gaussian noise process with time-varying phase, which makes it impossible to perform NF measurement through (7).

Compared with the first approach, the second technique can perform the phase and amplitude measurement almost simultaneously and does not have the constraints that the first approach has for the NF measurement. However, extra hardware to realize the division and sinusoidal operation shown in (8) is required.

A common problem associated with the first two approaches is that their amplitude calculation is based on the phase delay determined beforehand. So if there is any error in the phase delay calculation, the error will propagate to the subsequent amplitude calculation. However, the third approach doesn't have this drawback because the amplitude and phase are calculated independently through (6) and (10), but the cost is the extra hardware to implement the square and square root operations.

TABLE II
Pros and cons of the three approaches

Approach	#1	#2	#3
hardware overhead	Low	high	high
speed	Low	high	high
constraints	It cannot be used for NF Measurement.		no
propagation error	Yes	yes	no

The advantages and disadvantages of these three approaches are summarized in the Table II. The bold entries in the table are the desired properties for the ideal ORA. Through such a comparison, the third approach is seen to be the most preferred strategy. The only drawback of this approach is the extra hardware overhead. Because the amplitude is usually measured and evaluated in the unit of dB in real-life applications, the calculation of (10) can be transformed to the logarithm domain as

$$A'(\omega) = 20 \log_{10}(A(\omega)) = \frac{10}{\log_2 10} \log_2 (DC_1^2 + DC_2^2) \quad (11)$$

where $A'(\omega)$ is the measured amplitude in dB unit. The hardware implementation of (11) can be done with a LUT or simple linear approximation algorithm [8] depending on the precision requirement.

IV. EXPERIMENTAL RESULTS

We have implemented the BIST architecture shown in

Fig. 1 in hardware to perform the linearity, frequency response, and NF measurements. The digital portion of the BIST circuitry was implemented in a Xilinx Spartan XC2S50 FPGA on a Xilinx XSA50 printed circuit board (PCB). An 8-bit DAC with a low-pass filter and an 8-bit ADC were implemented on a separate PCB with a separate power supply. In this section, we present some experimental results to show the critical impact of phase delay on the measurement result obtained through the ORA.

A. Phase Delay Introduced by BIST Circuit

The sensitivity and accuracy of the measurements that can be obtained with this BIST approach can be particularly illustrated from a design error in the original BIST circuitry implemented in [1]. We found that there was an extra clock cycle delay in the path from the TPG, through MUX4 (see Fig. 1), to the ORA. Working in this mode, the BIST circuitry bypasses the DAC, DUT, and ADC totally and should introduce no phase delay. However, Fig. 3 shows a phase delay measured by the original BIST configuration in [1]. When the extra delay was removed, the phase response shown in Fig. 4 was obtained. Fig. 4 also illustrates that linear phase delay error is introduced by the ORA if the accumulation does not stop at an integer multiple of the period of the sine wave used to make the phase measurement. The reason is that the accumulation cannot totally cancel the non-DC signal shown as the “humps” in the curves of both Fig. 3 and Fig. 4.

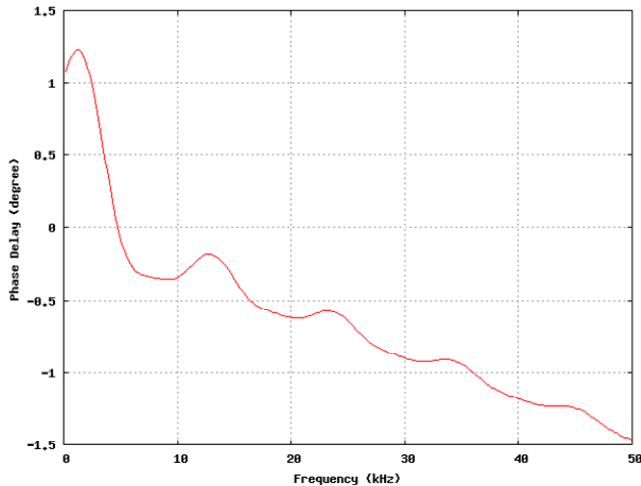


Fig. 3. Phase error due to delay introduced in TPG

While performing measurements on the DUT, the test signal must pass through the external path composed of the DAC with amplifier for low pass filter, the DUT and the ADC. So actually, the measured phase response is the total phase delay caused by all these four devices together. Therefore, the phase delay introduced by the DAC/ADC pair and amplifier also needs to be well calibrated out. Fig. 5 illustrates the impact of this kind of phase delay on the accuracy of the BIST circuitry. The reported phase response measured by the BIST circuitry in [1] shows an apparent error between the phase measurement done by original BIST

circuitry and the external test equipments and this error is drawn in Fig. 5. The other curve in the figure represents the phase delay caused by the DAC/ADC pair and Amplifier measured by modified BIST circuitry. Comparing these two curves, we can see that they are close to each other, which also shows that the phase delay in the DAC/ADC contributes to most of the phase measurement error in [1].

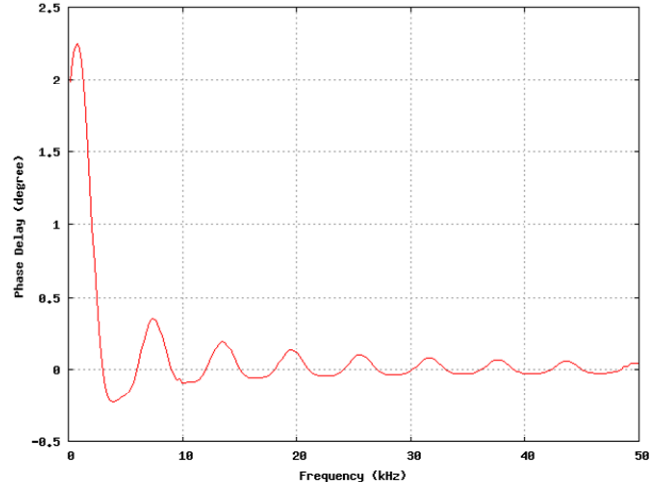


Fig. 4. Phase error with delay removed

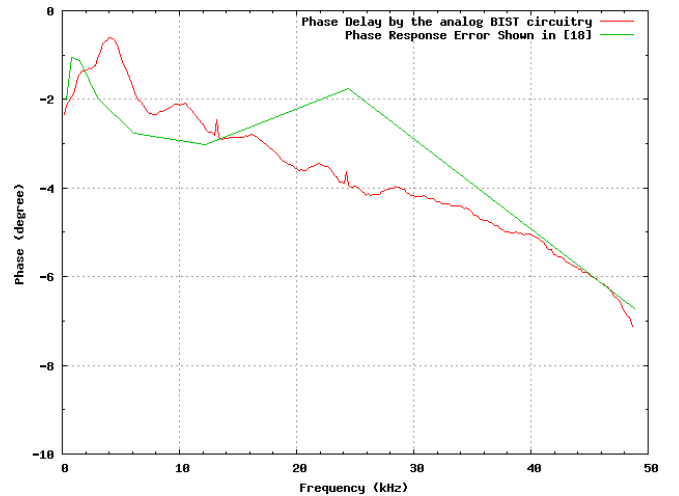


Fig. 5. Phase delay caused by DAC/ADC circuitry

B. Implementations of the MAC-based ORA

The MAC-based ORA was modeled in Verilog with parameterized number of input bits (N , which corresponds to the number of multiplier bits) and number of output bits (M , which corresponds the number of accumulator bits) to support the requirement for applications with varied bit-width. In our implementation, the BIST circuitry is synthesized into a Xilinx Spartan XC2S50 FPGA. Table III and IV summarize the resources required to implement the MACs as a function of different values for N and M .

As can be seen, when M increases, the logic required to realize the accumulator will increase correspondingly. Table III and Table IV show a linear relationship between the resource usage and M if N is fixed. In fact, the

accumulator requires exactly one slice for every two bits of the accumulator. However, the complexity of a multiplier increases much faster than an accumulator with increasing size, which is also illustrated by Table III and Table IV.

The MAC-based ORA can be also compared to the FFT-based BIST approach proposed in [7] and the FFT implementations in [9]. For a 256 point FFT with a 32 point approximate kernel, [7] used a XC2V8000, which itself is almost 250 times larger than the XC2S15 device, for implementation of that FFT-based BIST approach. The maximum clock frequency of that approach was reported to be between 1 and 2 MHz while our approach will operate at 48.5 MHz.

TABLE III
Number of slices vs. MAC configuration

	N=8	N=12	N=16
M=28	74	129	-
M=32	76	131	204
M=36	78	133	206
M=40	80	135	208
M=44	82	137	210

TABLE IV
Number of slices vs. MAC configuration

	N=8	N=12	N=16
M=28	139	244	-
M=32	143	248	387
M=36	147	252	391
M=40	151	256	395
M=44	155	260	399

TABLE V
RESOURCES USAGE OF 256-POINT FFT IMPLEMENTATIONS ON VIRTEX II

TYPE	# OF SLICES	# OF 18×18-BIT MULTIPLIERS	TRANSFORM FREQUENCY
Pipelined	2633	12	641 kHz
Burst I/O	2743	9	313 kHz
Minimum Resources	1412	3	133 kHz

[9] presents a number of FFT implementations for different point sizes on different series FPGAs. We chose three types of 256-point FFT implementations with 16-bit input implemented on a Xilinx Virtex II FPGA for comparison. The resources usage and performance of these implementations are summarized in Table V. Consider the fastest pipelined implementation in Table V as an example. With almost 7 times more slices and twelve 18-bit×18-bit multipliers (which, it should be noted, are not used in our BIST circuitry), the pipelined type FFT processor can only run at 641kHz. Furthermore, it should be noted that if we were to use the existing 18×18 multipliers in Virtex II for the multiplier in our MAC-based ORA, we would only require one multiplier and the number of slices needed for the accumulator is equal to M/2. As a result the largest configuration in Tables III and IV would only require one multiplier and 22 slices.

From such a comparison, we can conclude that the

MAC-based ORA is much simpler and cheaper, and can also achieve some flexibility that the FFT-based approach cannot provide. For example, the maximum number of the points that an FFT processor can compute is fixed, such that it is difficult to adjust the frequency resolution when using an FFT-based approach. Instead, the frequency resolution can be easily tuned with the step size of the sweeping frequency in our ORA. In addition, we are typically only interested in several frequency points or in a narrow bandwidth, which can be done easily using our ORA scheme while FFT-based scheme has to compute a great amount of information that may be useless because FFT processes the whole frequency domain at one time. The trade-off is in test time since the FFT can compute the entire frequency spectrum concurrently, while our MAC-based ORA measures one frequency component at a time.

V. CONCLUSIONS

In order to avoid the drawbacks associated with the conventional approaches to perform the mixed-signal testing and measurement, a BIST scheme has been proposed using a DDS-based TPG and a MAC-based ORA [1]. Both the theoretical analysis and experimental results from actual measurements show that the phase delay is very important to the implementation and accuracy of the MAC-based ORA. In comparison with the FFT-based approach, the MAC-based ORA can be realized using much more flexible and simpler BIST circuitry with less area penalty, which is what an ideal BIST scheme is supposed to be.

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