# Phase Delay in MAC-based Analog Functional Testing in Mixed-Signal Systems

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***Abstract:*** A Built-In Self-Test (BIST) approach has been proposed for functionality measurements of analog circuitry in mixed-signal systems. The BIST circuitry consists of a direct digital synthesizer (DDS) based test pattern generator (TPG) and multiplier/accumulator (MAC) based output response analyzer (ORA). In this paper we investigate and discuss the effects of phase delay on analog functionality measurements in mixed-signal systems when using MAC-based ORAs. We show that phase delay has a critical impact on the measurement results and that the MAC-based ORA is an effective method for measuring phase delay.

## 1. Introduction and Background

Mixed-signal Built-In Self-Test (BIST) is now in more demand than ever. First, the functionality test based on the traditional methodology of manual testing costs much more money and time due to the ever-increasing operational frequency and complexity of modern mixed-signal integrated circuits (ICs). For example, the RFIC test cost could be as high as 50% of the total cost, depending on the complexity of the functionality to be tested [1]. Therefore, it becomes attractive to automate the analog testing process with low-cost and built-in test circuitry. It is also most effective to consider testing in the product cycle as early as possible [2]. With properly designed BIST, the cost of added test hardware will be more than compensated for by the benefits in terms of reliability and the reduced testing and maintenance cost [3].

From the technological perspective, the increasing operational frequency and complexity of modern mixed-signal ICs make it very difficulty to perform test on these ICs. On one hand, with a rapidly increasing level of integration, the number of input/output (IO) pins does not increase accordingly. Thus, the observability of internal components is lower compared with traditional ICs [2]. On the other hand, the operational frequency of latest analog ICs at GHz requires tester electronics very close to the device under test (DUT), or even better, directly built on-chip [1]. Hence, BIST and other forms of embedded analog testing will eventually come to market [4].

In order to perform a suite of analog functionality tests, such as linearity, frequency response, and signal-to-noise ratio (SNR) measurements, in a BIST environment, the frequency spectrum of the signal coming from the device under test (DUT) needs to be measured and analyzed by an output response analyzer (ORA) included in the BIST circuitry. A few techniques were proposed to perform on-chip frequency-domain testing of mixed-signal circuits in [5]–[16]. However, all these techniques have associated disadvantages. For example, although [5]–[10] give some simple approaches aimed at decreasing the complexity of the embedded testing circuits, the precision provided by these approaches is limited. The on-chip linear ramp generators in [11]–[15] either depend heavily on the additional components, or have not been experimentally proven their fidelity. The approach in [16] based on Fast Fourier Transform (FFT) introduces considerable area overhead and power consumption to implemented on-chip test circuitry. Most of these approaches focus only on one or two simple parameter tests such as cut-off frequency of a filter and cannot perform complete analog tests such as frequency response, linearity, noise and modulation tests [1].

In order to avoid the drawbacks associated with the approaches mentioned in the previous paragraph, a new mixed-signal BIST approach has been proposed based on direct digital synthesizer (DDS) based test pattern generator (TPG) and multiplier/accumulator (MAC) based ORA [1][18]. A major merit of DDS is that its output frequency, amplitude, and phase can be precisely and rapidly manipulated under digital control. Other inherent DDS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly "hop" between frequencies [17]. Because the signal is in digital form, it is easy to include different modulation capabilities in the DDS. Therefore, many analog functional tests, such as magnitude and phase response in the frequency domain, 3rd order intercept point (IP3) and SNR can be performed in such an architecture [1]. On the other hand, in comparison with the FFT-based ORA which computes the spectrum over the whole frequency domain simultaneously, the MAC-based ORA only measures the spectrum at one frequency point at a time with the entire frequency spectrum obtained through successive measurements. Using such a scheme, the BIST hardware could be realized in a much simpler, cheaper and more flexible circuit.

In this paper, we discuss the effect of phase delay on the implementation and accuracy of the MAC-based

ORA. In addition, through the experimentation with the BIST circuitry, a simple comparison between the MAC-based ORA and FFT-based BIST scheme is also presented. The paper is organized as follows. Section 2 gives an overview of the BIST approach. This is followed by a detailed discussion of the effect of phase delay on the MAC-base ORA in Section 3. Some experimental results related to the MAC-based ORA are presented in Section 4 and the paper concludes in Section 5.

## 2. OVERVIEW OF BIST ARCHITECTURE

The mixed-signal BIST approach illustrated in Figure 1 is capable of accurate on-chip analog functional measurements for characterization and compensation of analog circuitry as well as for fault detection. In order to minimize the area and performance penalty on the analog circuitry, the majority of the BIST circuitry resides in the digital portion of the mixed-signal system. The digital portion of the BIST circuitry includes a DDS-based TPG, a MAC-based ORA, and a test controller. Locating the majority of the BIST circuitry in the digital portion of the mixed-signal system also provides an easy and efficient interface to the BIST circuitry for initiation of test and measurement sequences and retrieval of subsequent results by digital computing resources. The test scheme utilizes the existing digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) typically associated with most mixed-signal architectures to provide accurate analog testing and measurements while minimizing the hardware added for BIST.

The only test circuitry added to the analog domain is loopback capabilities needed to facilitate one or more return paths for the test signals to the ORA. The number and location of these loopback capabilities determines the accuracy and resolution of tests and measurements associated with a given analog function. For example, in Figure 1, the multiplexer labeled MUX4 facilitates testing and verification of the BIST circuitry prior to its use for test and measurement of the analog circuitry. The incorporation of MUX3 in the analog circuitry allows test and measurement of the DAC/ADC pair prior to test and measurement of the analog device under test (DUT). As a result, the effects of the DAC and ADC can be factored out for more accurate measurements of the DUT.

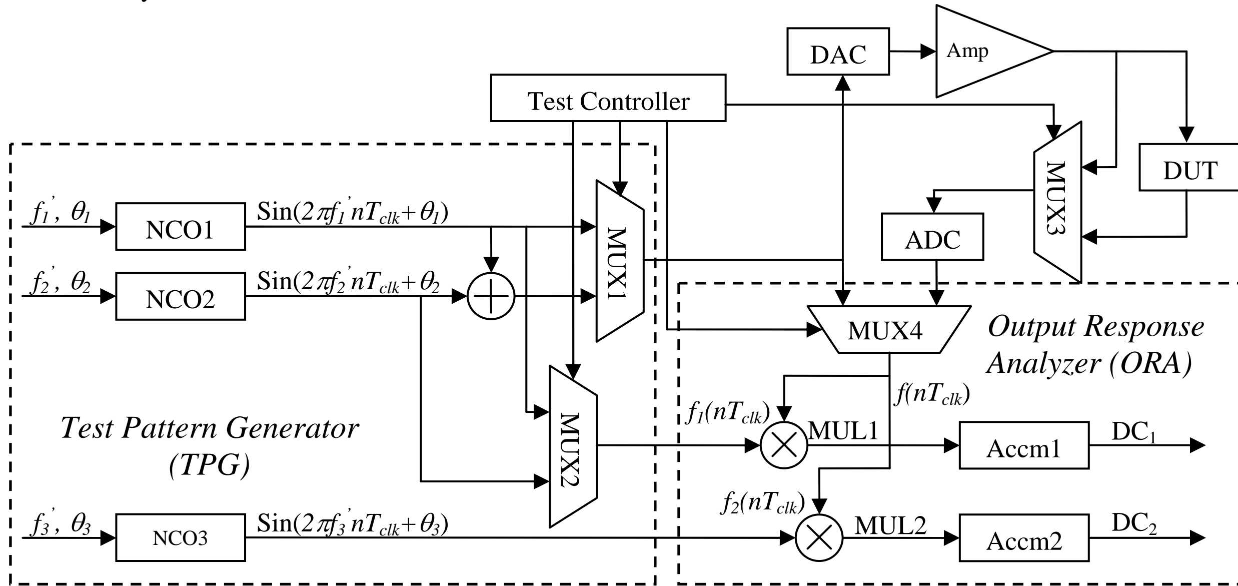


**Figure 1. General model of BIST architecture.**

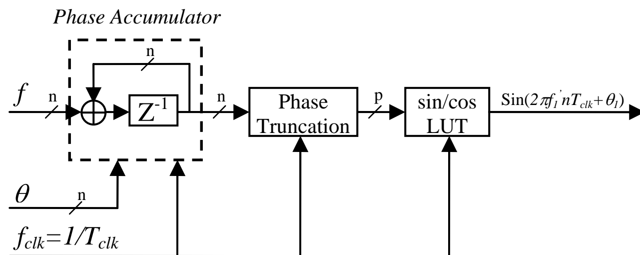


**Figure 2. NCO used in TPG.**

The DDS-based TPG consists of three numerically controlled oscillators (NCOs) and uses the existing DAC from the mixed-signal system to complete the DDS. The basic NCO used in the TPG to generate a sine wave in digital format is shown in Figure 2. The phase accumulator is used to generate the phase word based on the frequency word $f$ and the initial phase word $\theta$. Then the NCO utilizes a look-up table to convert the truncated phase word sequence to a digital sine wave

sequence shown in Figure 2. The output sine wave frequency is determined as

$$f' = \frac{f \cdot f_{clk}}{2^n}, \quad (1)$$

where $n$ is the word width of the phase accumulator. The phase truncation noise introduced in the NCO can be reduced using a sigma-delta modulator (SDM) [1]. The digital sine wave serves two purposes. One is to produce an analog signal, transformed from the digital sine wave through the DAC, to stimulate the DUT. The other purpose is to provide in-phase and out-of-phase test tones for the MAC-based ORA.

The ORA consists of two sets of $N \times N$-bit multiplier and $M$-bit accumulator pairs with each of the MACs performing in-phase and out-of-phase analysis, respectively. In the design of the ORA, $N$ is the number of bits from the DDS and ADC and $M$ is chosen such that $K<2^{M-2N}$, where $K$ is the length of the BIST sequence in clock cycles. A more detailed description of how the MAC-based ORA works is given in the following section.

### 3. Overview of Phase Delay

While performing the frequency response, linearity and SNR measurements, $f_1(nT_{clk})$ and $f_2(nT_{clk})$ (refer to Figure 1) is set to $cos(\omega nT_{clk})$ and $sin(\omega nT_{clk})$, respectively. As a result, the $DC_1$ and $DC_2$ accumulator values can be described as

$$DC_1 = \sum_n f(nT_{clk}) \cdot \cos(\omega nT_{clk}), \quad (2)$$

$$DC_2 = \sum_n f(nT_{clk}) \cdot \sin(\omega nT_{clk}) \cdot \quad (3)$$

From Equations (2) and (3), it can be seen that $DC_1$ and $DC_2$ are actually the in-phase and out-of-phase components of the signal $f(nT_{clk})$ at frequency $\omega$. Also the signal $f(nT_{clk})$'s Fourier Transform $F(\omega)$ can be expressed through $DC_1$ and $DC_2$ according to the following formula:

$$F(\omega) = \sum_n f(nT_{clk}) \cdot e^{j\omega nT_{clk}} = DC_1(\omega) + j \cdot DC_2(\omega) \cdot \quad (4)$$

From Equation (4), the signal $f_1(nT_{clk})$'s frequency spectrum—$F(\omega)$—within the bandwidth can be measured through the $DC_1$ and $DC_2$ by sweeping the frequency $\omega$ over the bandwidth of interest. However, in comparison with the FFT algorithm which computes $F(\omega)$ over the whole frequency domain simultaneously, the MAC-based ORA configuration in Figure 1 only measures $F(\omega)$ at one frequency point at a time with the entire frequency spectrum obtained through successive measurements.

From the above complex function $F(\omega)$, the amplitude $A(\omega)$ and the phase $\Delta\phi(\omega)$ of the spectrum $F(\omega)$ can be derived as follows:

$$F(\omega) = DC_1(\omega) + j \cdot DC_2(\omega) = A(\omega)e^{j\Delta\phi(\omega)}, \quad (5)$$

where

$$\Delta\phi(\omega) = tg^{-1}\frac{DC_2(\omega)}{DC_1(\omega)}, \quad (6)$$

$$\begin{aligned} A(\omega) &= F(\omega)e^{-j\Delta\phi(\omega)} \\ &= \sum_n f(nT_{clk}) \cdot e^{j[\omega nT_{clk} - \Delta\phi(\omega)]} \\ &= \sum_n f(nT_{clk}) \cdot \cos(\omega nT_{clk} - \Delta\phi(\omega)) \end{aligned}, \quad (7)$$

or

$$\begin{aligned} A(\omega) &= -j \cdot F(\omega)e^{j(\frac{\pi}{2} - \Delta\phi(\omega))} \\ &= -j \cdot \sum_n f(nT_{clk}) \cdot e^{j[\frac{\pi}{2} + \omega nT_{clk} - \Delta\phi(\omega)]} \\ &= \sum_n f(nT_{clk}) \cdot \sin(\frac{\pi}{2} + \omega nT_{clk} - \Delta\phi(\omega)) \end{aligned}. \quad (8)$$

These two parameters are used much more widely in functional measurements of analog circuits. The amplitude response $A(\omega)$ is of interest to functional measurements because many important parameters, such as cut-off frequency, in-band ripple, bandwidth, signal-to-noise ratio, etc., are determined by it. The phase response $\Delta\phi(\omega)$ is also called as group delay, which can be used to describe the delay introduced by electrical devices. It is because of the phase delay that there is normally a phase difference between the external path through the DUT and the internal path from the TPG to the ORA (refer to Figure 1).

The phase delay is an important issue to the MAC-based ORA because it will affect the accuracy and implementation of the BIST approach. Once the phase retardation $\Delta\phi(\omega)$ is identified based on the Equation (6), $A(\omega)$ can be measured through $DC_2$ or $DC_1$ according to Equations (7) or (8) if the test tone generated by NCO can be phase-adjusted using $\Delta\phi(\omega)$ or $\pi/2-\Delta\phi(\omega)$. However, once we have obtained $\Delta\phi(\omega)$ from Equation (6), we can also correct the measured magnitude $A(\omega)$ as follows:

$$A(\omega) = \frac{DC_1}{\cos\Delta\phi(\omega)} = \frac{DC_2}{\sin\Delta\phi(\omega)} \quad (9)$$

Therefore, the technique measures not only the phase difference, but also facilitates correction of the gain measurement based on the phase difference. This ensures the accuracy of the proposed BIST scheme for

linearity, frequency response, and SNR measurements. Accurate measurement of the phase delay is therefore critical to the functionality measurements made by the MAC-based ORA.

For an on-chip test, we don't have to set up a full-length *arctan* look-up table (LUT) to get the exact phase delay from $DC_1$ and $DC_2$. First the quadrant of $\Delta\phi(\omega)$ can be determined easily from the sign bits of $DC_1$ and $DC_2$. Before we further the discussion, we define a new term, the *absolute phase offset* of $\Delta\phi(\omega)$ in the corresponding quadrant, to simplify the analysis. The *absolute phase offset* $\Delta\phi_o(\omega)$ can be calculated through the formula as

$$\Delta\phi_o(\omega)=\begin{cases} tg^{-1}\dfrac{|DC_2(\omega)|}{|DC_1(\omega)|} & |DC_1(\omega)|\ge|DC_2(\omega)| \\ tg^{-1}\dfrac{|DC_1(\omega)|}{|DC_2(\omega)|} & |DC_1(\omega)|\ge|DC_2(\omega)| \end{cases} \quad (10)$$

From the Equation (10), we can find out that the value range of $\Delta\phi_o(\omega)$ varies from $0^\circ$ to $45^\circ$. Also the relationship between the phase delay $\Delta\phi(\omega)$ and the absolute phase offset $\Delta\phi_o(\omega)$ can be shown in Table 1.

**Table 1. Relationship between $\Delta\phi(\omega)$ and $\Delta\phi_o(\omega)$**

| | **$\lvert DC_1\rvert \ge \lvert DC_2\rvert$** | **$\lvert DC_1\rvert \le \lvert DC_2\rvert$** |
|---|---|---|
| **$DC_1>0$; $DC_2>0$** | $\phi(\omega)=\Delta\phi_o(\omega)$ | $\Delta\phi(\omega)=90^\circ-\Delta\phi_o(\omega)$ |
| **$DC_1>0$; $DC_2<0$** | $\phi(\omega)=360^\circ-\Delta\phi_o(\omega)$ | $\Delta\phi(\omega)=270^\circ+\Delta\phi_o(\omega)$ |
| **$DC_1<0$; $DC_2>0$** | $\phi(\omega)=180^\circ-\Delta\phi_o(\omega)$ | $\Delta\phi(\omega)=90^\circ+\Delta\phi_o(\omega)$ |
| **$DC_1<0$; $DC_2<0$** | $\phi(\omega)=180^\circ+\Delta\phi_o(\omega)$ | $\Delta\phi(\omega)=270^\circ-\Delta\phi_o(\omega)$ |

Therefore, the $\Delta\phi(\omega)$ can be identified with $\Delta\phi_o(\omega)$ whose value range is $[0^\circ, 45^\circ]$. Upon the analysis until now, the *arctan* look-up table (LUT) can be decreased by half. However, when $DC_2/DC_1$ is very small, the *arctan*($DC_2/DC_1$) can be represented by the ratio of the $DC_2/DC_1$. So the length of the *arctan* look-up table (LUT) can be compressed further such that the hardware resources used by the phase calculation can be minimized while keeping the calculation result precise enough.

As implied above, there are at least two techniques for compensating for the phase delay to prevent seriously degrading the accuracy of the amplitude measurement. One approach is to adjust the phase of the outgoing test tone in the NCO such that the DUT output is in phase with the signal to be mixed in the MAC-based ORA and then make the amplitude measurement. The other approach is to calculate the corrected amplitude directly from Equation (4). A third approach is to obtain the amplitude directly from $DC_1$ and $DC_2$ without a phase delay measurement as follows:

$$A(\omega)=\sqrt{DC_1^2+DC_2^2} \quad (11)$$

All these three approaches have their own advantages and disadvantages. The most attractive merit of first approach is that it doesn't require any extra circuitry to calculate the amplitude once the phase delay is identified. Such a simple hardware implementation is what we expect from a good BIST strategy. However, there are also some disadvantages associated with this approach. First, an extra accumulation cycle is required to obtain the amplitude response, which will definitely slow down the processing speed. Second, this approach cannot be used for SNR measurement. In the linearity and frequency response measurements, all the signals under analysis by the ORA are deterministic signal, which means the phase delay is a constant. So once the phase delay is identified in one accumulation cycle, the phase delay can be used in the subsequent accumulation cycle. However, the situation differs in the SNR measurement. Usually the noise in electric devices can be modeled as a white Gaussian noise process whose phase also varies from time to time and need be viewed as a random variable. In other words, the phase delay keeps changing in different accumulation cycles. Therefore, the SNR measurement cannot be performed through Equations (7) and (8).

Compared with the first approach, the second one can perform the phase and amplitude measurement almost at the same time. Also it does not have the constraints that the first approach does for the SNR measurement. However, extra hardware to realize the division and sinusoidal operation shown in Equation (9) is required in this approach.

There is one common point between the first two approaches that the amplitude is calculated based on the phase delay obtained beforehand. So if there is any calculation error in the phase delay, the error will be definitely introduced into the calculation of amplitude and degrade the precision. The third approach doesn't have this drawback because the amplitude and phase are calculated independently according to the Equation (6) and (11), but the cost is the extra hardware to implement the square and square root operations.

The advantages and disadvantages of these three approaches are summarized in the Table 2. The highlight part in the table is the desired properties which we want for an ideal ORA implementation. Through such a comparison, the third approach is the most preferred strategy which should be used in the ORA implementation. The only drawback of this approach is the extra hardware introduced by the square root operation. Because the amplitude is usually measured and evaluated in the unit of dB in real-life applications, the calculation of the Equation (11) can be transformed to the logarithm domain as

$$A^{'}(\omega) = 20\log_{10}(A(w)) = \frac{10}{\log_2 10}\log_2(DC_1^2 + DC_2^2) \quad (12)$$

where $A^{'}(\omega)$ is the measured amplitude in dB unit. The hardware implementation of the Equation (12) can be done with LUT or simple linear approximation algorithm [19] depending on the precision requirement.

**Table 2. Pros and cons of the three approaches**

| Approach | # 1 | # 2 | # 3 |
|---|---|---|---|
| **hardware overhead** | **Low** | high | high |
| **speed** | Low | **high** | **high** |
| **constraints** | It cannot be used for SNR Measurement. | **no** | **no** |
| **propagation error** | Yes | yes | **no** |

## 4. EXPERIMENTAL RESULTS

We have implemented the BIST architecture shown in Figure 1 in hardware to perform the linearity, frequency response, and SNR measurements of analog circuitry. The digital portion of the BIST circuitry was implemented in a Xilinx Spartan XC2S50 FPGA on a Xinlix XSA50 printed circuit board (PCB). An 8-bit DAC with low-pass filter and an 8-bit ADC were implemented on a separate PCB with a separate power supply. In this section, we will present some experimental results to show the critical impact of phase delay on the measurement result obtained through the MAC-based ORA.

### *A. Phase Delay Introduced by BIST Circuit*

The sensitivity and accuracy of the measurements that can be obtained with this BIST approach can be particularly illustrated from a design discrepancy in the original BIST circuitry implementation in [18]. Recently we found that there was an extra clock cycle delay in the path from the TPG, through MUX4, to the ORA (refer to Figure 1). Working in this mode, the BIST circuitry bypasses the DAC, DUT, and ADC totally and should introduce no phase delay. However, Figure 3 shows a phase delay response measured by the original TPG and ORA configuration in [18]. When the extra clock cycle of delay was removed, the phase response shown in Figure 4 was obtained. Note that Figure 4 not only shows the elimination of the phase error as a result of the corrected BIST circuit design but also shows that the phase error decreases as the number of accumulation cycles in the ORA increases. However, Figure 4 also illustrates that linear phase delay error is introduced in the measurement by the ORA if the accumulation does not stop at an integer multiple of the period of the sine wave used to make the phase measurement. Otherwise, the accumulation in the ORA cannot totally cancel the non-DC signal as shown by the "humps" in the curves of both Figure 5 and Figure 6. It should be noted that data in Figure 5 and Figure 6 were obtained directly from our experimental BIST hardware and illustrates the accuracy of the phase delay measurements made with the BIST circuitry.

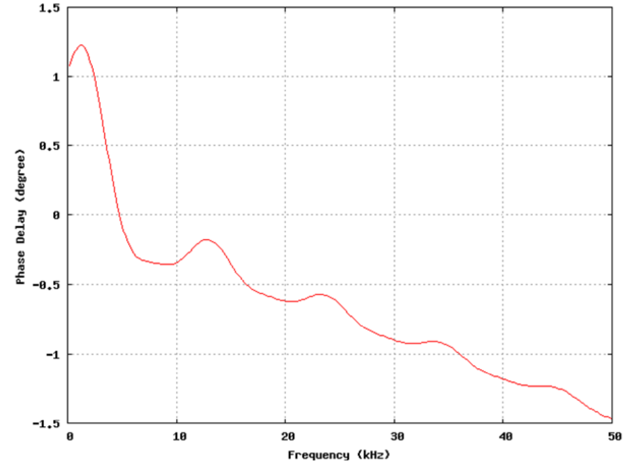


**Figure 3. Phase error due to delay introduced in TPG**

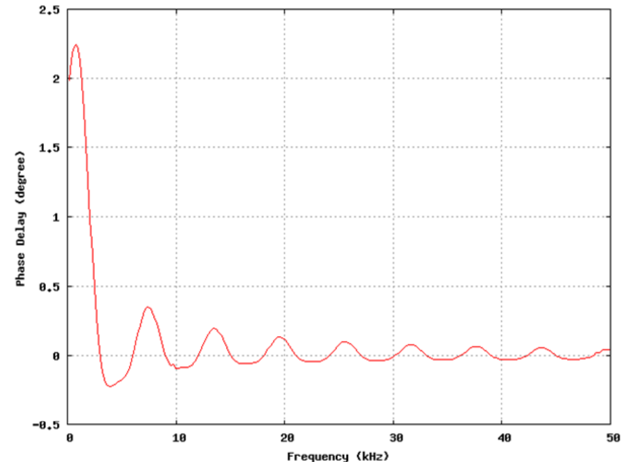


**Figure 4. Phase error with delay removed**

Even after the phase delay caused by the digital circuitry is perfectly balanced out, the measurement still detects the phase delay introduced by the ADC/DAC pair and Amplifier. While performing measurements on the DUT, the test signal must pass through the external path composed of ADC, Amplifier, DUT and DAC (refer to Figure 1). So actually, the measured phase response is the total phase delay caused by all these four electric devices together. Therefore, the phase delay introduced by the DAC/ADC pair and Amplifier also needs to be factored out, otherwise the accuracy of the DUT measurements may suffer. Figure 5 illustrates the impact of this kind of phase delay to the sensitivity and accuracy of the BIST circuitry. The reported phase response measured by the BIST circuitry in [18] shows an apparent error between the BIST measured phase re-

sponse and the actual measurement using the external test equipments. This error is shown in one of the curves in Figure 5. The other curve represents the phase delay caused by the DAC/ADC pair and Amplifier which is measured through the external path that passes through the DAC/ADC pair and Amplifier and bypasses the DUT at the same time. Comparing these two curves, we can see that these two curves are very close to each other, which also means the phase delay in the DAC/ADC and Amplifier contributes to most of the phase measurement error shown in [18].

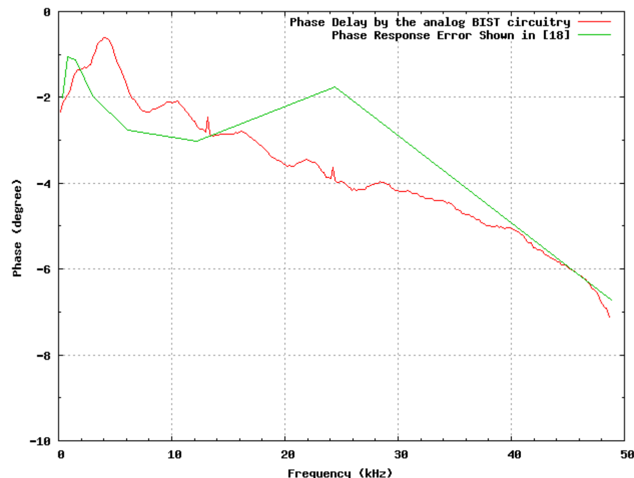


**Figure 5. Phase delay caused by DAC/ADC circuitry**

### *B. Implementations of the MAC-based ORA*

The proposed BIST scheme is intended to be a comprehensive solution which can serve for various mixed-signal systems. Usually different systems use ADCs with different resolution. So the MAC-based ORA must be modeled with parameterized number of input bits (*N*, which corresponds to the number of multiplier bits) and number of output bits (*M*, which corresponds the number of accumulator bits) to support the requirement for tested signal with varied bit-width. Recall from the earlier discussion that in the design of the ORA, *N* is the number of bits from the DDS and ADC and *M* is chosen such that $K<2^{M-2N}$, where *K* is the desired length of the BIST sequence in clock cycles.

In our implementation, the BIST circuitry is synthesized into a Xilinx Spartan XC2S50 FPGA. Table 3 and Table 4 summarize the resources, in terms of the number of slices and number of look-up tables (LUTs), respectively, required to implement the MACs as a function of different values for the number of input bits, *N*, and the number of output bits, *M*.

As can be seen, when the output bit number increases, the logic required to realize the accumulator will increase correspondingly. Table 3 and Table 4 show a perfect linear relationship between the used resources and the MAC's output bit width if the input bit width is fixed. In fact, the accumulator requires exactly one slice for every two bits of the accumulator. However, the complexity of a multiplier increases much faster than an accumulator with the increasing size, which is also well illustrated by Table 3 and Table 4. It should be noted that the MAC with 16-bit input and 28-bit output is not evaluated because the 32-bit output of a 16-bit multiplier multiplier is wider than the accumulator in such a MAC. Therefore, it does not make any sense to consider this case.

**Table 3. Number of slices vs. MAC configuration**

| | | # OF INPUT BITS, N | | |
|---|---|---|---|---|
| | | **8** | **12** | **16** |
| # OF OUTPUT BITS, M | **28** | 74 | 129 | - |
| | **32** | 76 | 131 | 204 |
| | **36** | 78 | 133 | 206 |
| | **40** | 80 | 135 | 208 |
| | **44** | 82 | 137 | 210 |

**Table 4. Number of LUTs vs. MAC configuration**

| | | # OF INPUT BITS, N | | |
|---|---|---|---|---|
| | | **8** | **12** | **16** |
| # OF OUTPUT BITS, M | **28** | 139 | 244 | - |
| | **32** | 143 | 248 | 387 |
| | **36** | 147 | 252 | 391 |
| | **40** | 151 | 256 | 395 |
| | **44** | 155 | 260 | 399 |

The MAC-based ORA can be also compared to the FFT-based BIST approach proposed in [16] and the FFT implementations in [20]. For a 256 point FFT with a 32 point approximate kernel, [16] used a Virtex II XC2V8000, which itself is almost 250 times larger than the XC2S15, for implementation of that FFT-based BIST approach. The maximum clock frequency of this approach was reported to be between 1 and 2 MHz while our approach will operate at 48.5 MHz with no modifications to the architecture, such as pipelining, to improve performance [18].

As a further comparison, reference [20] gives a number of FFT implementations for different point size on Virtex-II, Virtex-II Pro, Spartan-3E, and Virtex-4 series FPGAs. We chose three types of 256-point FFT implementations with 16-bit input on Virtex II for comparison. The resources usage and performance of these implementations in a Virtex-II FPGA are summarized in Table 5.

Consider the fastest pipelined implementation in Table 5 as an example. With almost 7 times more slices and twelve 18-bit×18-bit multipliers that are not used in our circuitry, the pipelined type FFT processor can only run at 641kHz. Furthermore, it should be noted that if

we were to use one of the existing 18×18 multipliers in Virtex II for the multiplier in our MAC-based ORA, the number of slices needed for the accumulator is equal to $M/2$ (since two accumulator bits can be implemented in a single slice). As a result the largest configuration in Tables 3 would require one multiplier and 22 slices.

**Table 5. Resources usage of 256-point FFT implementations on Virtex II FPGAs**

| TYPE | # OF SLICES | # OF 18×18-BIT MULTIPLIERS | TRANSFORM FREQUENCY |
|---|---|---|---|
| Pipelined | 2633 | 12 | 641 kHz |
| Burst I/O | 2743 | 9 | 313 kHz |
| Minimum Resources | 1412 | 3 | 133 kHz |

From such a comparison, we can conclude that the MAC-based ORA is much simpler and cheaper, and can also achieve some flexibility that the FFT-based approach cannot provide. For example, the maximum number of the points that an FFT processor can compute is fixed, such that it is difficult, if not impossible, to adjust the frequency resolution when using an FFT-based approach. Instead, the frequency resolution can be easily tuned with the step size of the sweeping frequency in our ORA. In addition, we are typically only interested in several frequency points or in a narrow bandwidth, which can be done easily using our ORA scheme while FFT-based scheme has to compute a great amount of information that may be useless because FFT processes the whole frequency domain at one time.

## 5. CONCLUSIONS

In order to avoid the drawbacks associated with the conventional approaches to perform the mixed-signal testing and measurement, a BIST scheme has been proposed based on a DDS-based TPG and a MAC-based ORA [1][18]. Both the theoretical analysis and experimental results from actual measurements show that the phase delay is very important to the implementation and accuracy of the MAC-based ORA. In comparison with the FFT-based approach, the MAC-based ORA can be realized using much more flexible and simpler BIST circuitry with less area penalty, which is what an ideal BIST scheme is supposed to be.

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