

FPGAs: Excellent Platforms for SoC Testing R&D

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Abstract

Incorporation of complex embedded cores including programmable multi-port memories, digital signal processors (DSPs), and clock management systems, makes field programmable gate arrays (FPGAs) more closely resemble system-on-chip (SoC) implementations. As a result, FPGA testing techniques are not only increasing in scope, but are becoming increasingly important for a broader range of system applications. FPGA testing challenges continue to increase with the introduction of new cores and architectures as a result of their complex programmable functionality and limited implementation information in datasheets. Yet, these testing challenges in conjunction with the programmability of FPGAs provide excellent platforms for research and development of new SoC test architectures, strategies, and methodologies.

1. Introduction

During the development of Built-In Self-Test (BIST) for Xilinx Virtex-4 and Virtex-5 FPGAs¹, a number of cases were encountered where testing specialized embedded cores required considerable investigation and evaluation of both classic and new testing techniques. The following examples include error-correcting codes (ECC) in RAM cores and multipliers and adders in DSP cores.

2. ECC RAMs

The ECC RAMs in Virtex-4 use Hamming code to identify correctable single bit errors and non-correctable double bit errors. The Hamming code generator, checker, and bit error correction circuitry is made almost exclusively of XOR gates. Yet there is little information on the actual implementation of these circuits in the datasheets and application notes for these FPGAs. Fortunately, some classic work in testing XOR-based parity circuits [1][2] led to a generalized approach to test ECC RAMs, details of which can be found in Chapters 3 and 12 of [3].

3. DSP Multipliers and Adders

The DSP cores in Virtex-4 primarily consist of an 18×18-bit multiplier and a 3-port adder/subtractor implementing $Z_{\pm}(X+Y+C_{in})$, where X, Y, and Z are the three ports to the adder [4]. The X and Y ports of the adder are used to sum the two partial products produced by the multiplier. Based on analysis of the limited information in datasheets and application notes, the multiplier is assumed to be a

modified-Booth/Wallace tree (with the final stage adder removed) and the 3-port adder/subtractor is assumed to be a 2-stage carry look-ahead adder (CLA).

Some of the classic work in BIST for modified-Booth and Booth/Wallace tree multipliers includes [5] and [6]. Both approaches use an 8-bit counter to test an N -bit multiplier. In [5], the 4 MSBs of the counter drive one port of the multiplier while the 4 LSBs drive the other port, replicating the bits as need to reach N bits. In [6], higher fault coverage was obtained by using the 5 MSBs to drive the Booth encoding port of the multiplier while the 3 LSBs drive the other port. Unfortunately, the Booth encoding port is not specified in the literature. When we performed fault simulation, we found that running the BIST sequence twice and swapping the ports provided even higher fault coverage than that reported in [6].

An excellent BIST approach for CLAs is reported in [7] where an $N+1$ -bit ring (TR) counter in conjunction with N XOR and N XNOR gates is used to test an N -bit CLA. When we performed fault simulation, we found that two test patterns were missing for complete fault detection. However, these two vectors are obtained by replacing the inverter in the TR counter with an inverting flip-flop, such that the TR counter is $N+2$ bits. Furthermore, we found that 100% single stuck-at fault coverage is obtained for any CLA architecture (ripple CLA, ripple look-ahead carry unit (LCU), or multi-stage LCU). This approach facilitates testing the 3-port adder/subtractor one stage at a time.

4. References

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