



Analog Frequency Response Measurement in Mixed-Signal Systems

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Abstract—We present an efficient approach for on-chip frequency response measurement, including phase and gain, of analog circuitry in mixed-signal systems. The approach uses direct digital synthesizer (DDS) to supply test sine waves with different frequencies and phases. The output response is analyzed using a multiplier and accumulator. The resultant phase delay measurement is used to correct other measurements such as gain and linearity for more accurate testing and characterization of the analog circuit under test. The approach was implemented in Verilog, synthesized in a Field Programmable Gate Array (FPGA), and used for frequency response measurements of an actual device under test.

I. INTRODUCTION

We have developed a Built-In Self-Test (BIST) approach capable of on-chip functional measurements including linearity and frequency response [1]. The test pattern generator (TPG) uses a direct digital synthesizer (DDS) which can generate a variety of modulated waveforms and frequency tones for analog functional test. The output response analyzer (ORA) consists of a multiplier and an accumulator which is capable of measuring the power of an analog output response waveform at any desired frequency. The majority of the BIST circuitry resides in the digital portion of the mixed-signal system to minimize the area and performance impact on the analog circuitry. The only test circuitry added to the analog domain is a return path for the test signals to the ORA portion of the BIST circuitry. The BIST approach utilizes the existing digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) typically associated with conventional duplex mixed-signal architectures and thus provides accurate analog circuitry testing without adding much extra hardware. This TPG and ORA combination lead to an efficient BIST approach that we have been investigating and analyzing for its ability to assist in characterization and calibration during manufacturing and field testing. A major problem encountered is the effect of phase delay on measurements made with the multiplier/accumulator-based ORA [2]. This leads to inaccuracy in measuring gain, linearity, signal-to-noise ratio, etc. The solution proposed in [2] is effective but requires a considerable amount of additional hardware in the BIST circuitry and additional testing time.

In this paper, we show that the phase delay can be measured

and the problem solved with no additional hardware than that originally proposed in [1]. We begin with an overview of the DDS and DDS-based BIST approach in Section II. In Section III we discuss the problem of the phase delay in frequency response measurements where we also present a new and efficient solution to measure and compensate for phase delay in both frequency response and linearity measurements. We present experimental results in Section IV and conclude the paper in Section V.

II. OVERVIEW OF BIST APPROACH

DDS is a frequency synthesis technique that provides fast and precise frequency test tones. As shown in Figure 1, a conventional DDS includes a digital accumulator that generates the phase word based on the input frequency word F_r . The synthesizer step size is defined as $f_{clk}/2^n$ where n is the number of bits in the frequency word F_r . Fine resolution can thus be achieved using frequency word with a large number of bits n and this would also lead to a large accumulator size. The DDS utilizes a ROM look-up table composed of sine wave information to convert the phase word to a sinusoidal amplitude word. The amplitude word length is limited by the DAC resolutions (D bits).

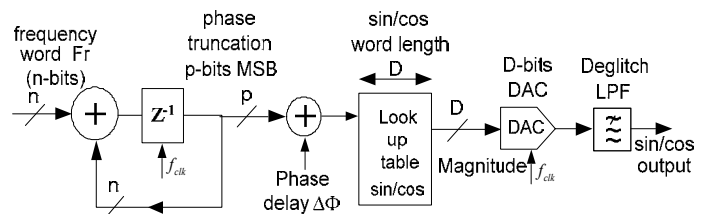


Figure 1. DDS for test tone generation.

The TPG and ORA are illustrated in Figure 2 in the BIST for the analog frequency response measurement architecture. The DDS-based TPG provides a precise frequency tone sweep by sweeping the frequency word F_r . It also can generate 4 quadrant sine waveforms simultaneously by shifting the 2 MSBs of the phase word. The area penalty associated with the DDS approach is minimized by the delta-sigma noise shaping scheme [1].

The ORA consists of a D -bit multiplier (where D is the number of bits from the ADC) and a $2D+M$ -bit accumulator (where the number of samples to be accumulated is less than 2^M). A 2's

complement transformation is performed on negative numbers entering Accumulator3 and Accumulator4 such that subtraction is accomplished by the adders in the accumulators. In addition, the DDS input to the two multipliers is converted to a signed magnitude number to remove DC offset from the DDS output. The sign bit is then used to control the 2's complement transformation at the input to the accumulators [2].

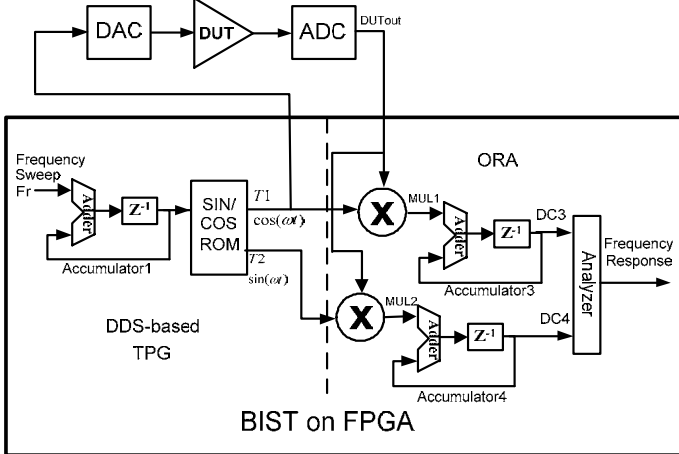


Figure 2. Frequency response BIST measurement.

III. FREQUENCY RESPONSE TEST

One of major problems associated with integrated analog circuitry such as filters and amplifiers is the cutoff frequency variation due to temperature, supply voltage and process variations. If the cut-off frequency can be monitored on the fly during transmission idle periods (e.g., the preamble period in WLAN applications), its variation can be compensated using built-in tunable circuitry in analog designs. In addition to production test, the frequency response monitoring can also be used to adjust the gain and bandwidth of the analog circuitry for multi-band and multi-standard applications. With wireless standards operating in very different frequency bands, market-leading wireless solutions have to offer multi-mode interoperability with transparent worldwide usage. Thus, the base-band gain stage needs to be tunable for different wireless standards. The BIST approach can be used to calibrate the frequency response of the base-band gain stage in this connection.

Frequency response (both amplitude and phase response) is the key measure for integrated filters and amplifiers. The commonly interested cut-off frequency of the filters and amplifiers can be found by measuring the passband and stopband amplitude response, while the linearity (group delay) can be determined from the phase response. The DDS generates frequency tones that can scan the pass and stop bands of the device under test (DUT) with fine steps and can thus measure the passband and stopband ripples. An amplifier frequency response measure by DDS test tones is illustrated in Figure 3. However, since there is normally a phase

delay $\Delta\phi$ between the external path through the DUT and the internal path from the test generator to the test analyzer, phase correction needs to be done prior to the frequency magnitude measurement.

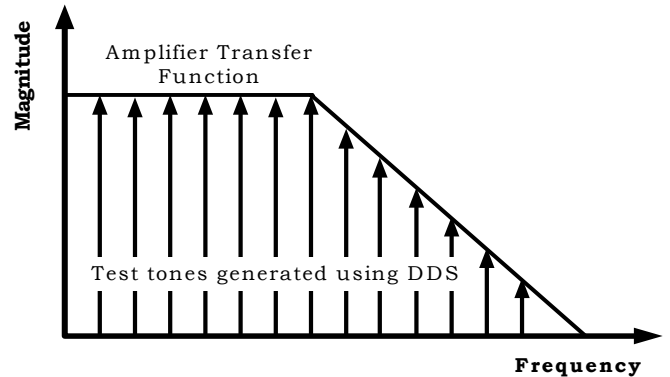


Figure 3. Frequency response test using DDS.

During a specific frequency sweep period, the DDS-based TPG generates two test signals with same amplitude and frequency but with a 90° phase shift: $T_1 = A \cos \omega_1 t$ and $T_2 = A \sin \omega_1 t$. After the test signal T_1 passes through the DUT, both its amplitude and phase will change. The signal at DUT's output is thus given by:

$$DUTout = A_1 \cos(\omega_1 t - \Delta\phi_1) + k \quad (1)$$

where A_1 and $\Delta\phi$ represent the amplitude and phase delay of the DUT at the frequency ω_1 and k is a DC offset.

In the ORA, the $DUTout$ is multiplied separately by T_1 and T_2 and their outputs are MUL1 and MUL2:

$$MUL1 = A \cos(\omega_1 t) \cdot (A_1 \cos(\omega_1 t - \Delta\phi_1) + k) \quad (2)$$

$$= \frac{AA_1}{2} [\cos \Delta\phi_1 + \cos(2\omega_1 t - \Delta\phi_1)] + Ak \cos \omega_1 t$$

$$MUL2 = A \sin(\omega_1 t) \cdot (A_1 \cos(\omega_1 t - \Delta\phi_1) + k) \quad (3)$$

$$= \frac{AA_1}{2} [\sin \Delta\phi_1 + \sin(2\omega_1 t - \Delta\phi_1)] + Ak \sin \omega_1 t$$

We accumulate MUL1 and MUL2 and end the accumulations at a same accumulation cycle N . The accumulated results are:

$$DC_3 \approx \frac{1}{2} AA_1 \cos \Delta\phi_1 \cdot N \quad (4)$$

$$DC_4 \approx \frac{1}{2} AA_1 \sin \Delta\phi_1 \cdot N \quad (5)$$

Thus, the phase delay $\Delta\phi_1$ can be determined by

$$\Delta\phi_1 = \arctan\left(\frac{DC_4}{DC_3}\right) \quad (6)$$

Once the phase delay is measured, the test tone for frequency response generated by DDS can be phase-adjusted such that the signals at the mixer inputs can be perfectly in-phase. In this

connection, DDS should generate test tones in form of $T_3=A\cos(\omega t-\Delta\phi)$ for DUT and $T_1=A\cos(\omega t)$ for the mixer input in the ORA, respectively. Additional phase can be easily added to the phase word in the DDS architecture as shown in Figure 1. Since the DUT may not have a constant phase delay, namely, the delay through the DUT is normally frequency-dependent, the phase correction should be performed at each frequency step when DDS generates the test tones that scan the interested band.

Figure 4 shows the ORA accumulated results DC_3 , DC_4 from ORA to test a DUT with a phase delay $\Delta\phi=135^\circ$ in MatLab. Notice the slope of DC_3 is negative due to the $\cos\Delta\phi$ term in (4), while the slope of DC_4 is positive due to the $\sin\Delta\phi$ term in (5). Based on the sign of DC_3 and DC_4 , we can thus determine the quadrant of the phase delay. Therefore, once the phase delay is determined, the actual phase corrected amplitude response can be found from either DC_3 or DC_4 measurements as follows:

$$DC = \frac{DC_3}{\cos \Delta\phi} = \frac{DC_4}{\sin \Delta\phi} = \frac{1}{2} AA_1 \cdot N \quad (7)$$

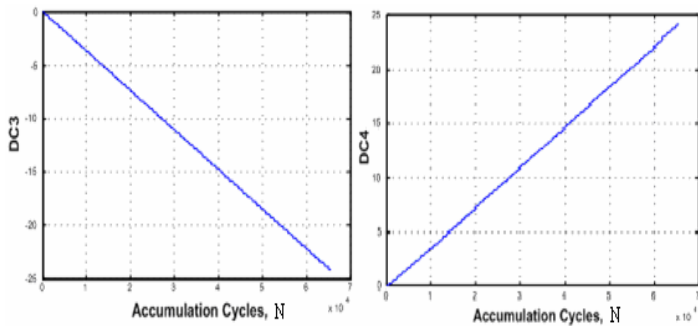


Figure 4. Simulated DC_3 , DC_4 of DUT with phase delay $\Delta\phi=135^\circ$.

Therefore, the phase delay can be not only be measured, but the amplitude can be correct in a single test. As a result there is no need to adjust the phase to the DDS and repeat the test sequence with the adjusted phase delay as was proposed in [2]. For on chip test, we don't have to set up an arctan table to get the exact phase delay from DC_3 and DC_4 . As discussed before, the quadrant of $\Delta\phi$ can be determined easily by the sign bits of DC_3 and DC_4 . The ratio of the DC_4/DC_3 can represent the $\arctan(DC_4/DC_3)$ when DC_4/DC_3 is very small. For large DC_4/DC_3 , the phase delay can be represented by $\arctan(DC_4/DC_3) = \pi/2 - DC_3/DC_4$. For $DC_4/DC_3 \approx 1$, adjustments can be made to get approximate value of phase delay $\Delta\phi$.

IV. EXPERIMENTAL RESULTS

We have implemented the BIST approach in hardware to obtain frequency response measurements of analog circuitry. A first order low pass filter was built as the DUT. A 12-bit DAC with low-pass filter and a 12-bit ADC were implemented on a separate printed circuit board with a separate power supply but only the

eight most significant bits of the DAC and ADC were used in our system to demonstrate a BIST scheme with small area penalty. The digital BIST circuitry was implemented in a Xilinx Spartan 2S50 FPGA on a Xess XSA50 printed circuit board. Figure 5 shows the measured DC_3 and DC_4 outputs using BIST at a test input frequency of 48.8KHz. The phase delay measured by BIST is 79° and matches closely with the measurement taken from an oscilloscope. Figure 6 and Figure 7 show the BIST measured frequency response of the filter (phase and amplitude, respectively) after running the whole frequency sweep test compared to the actual measurements in the lab using an oscilloscope.

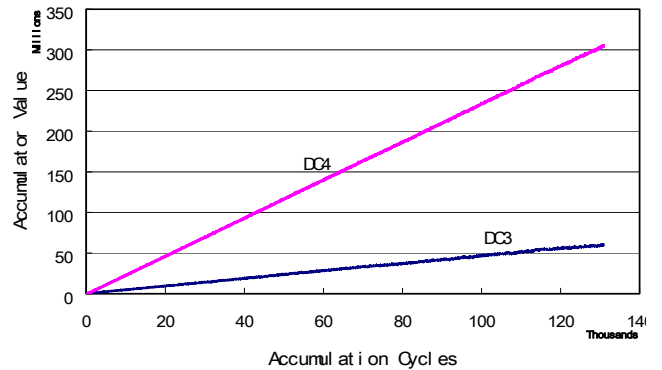


Figure 5. Actual BIST circuit accumulated DC_3 and DC_4 for a phase delay $\Delta\phi \approx 79^\circ$.

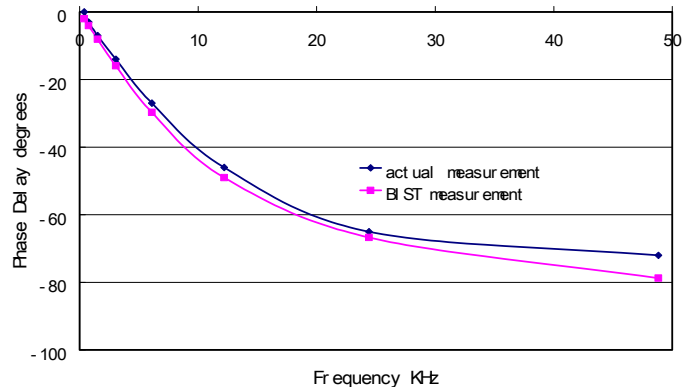


Figure 6. BIST measured phase response and actual measurement of 1st order LPF.

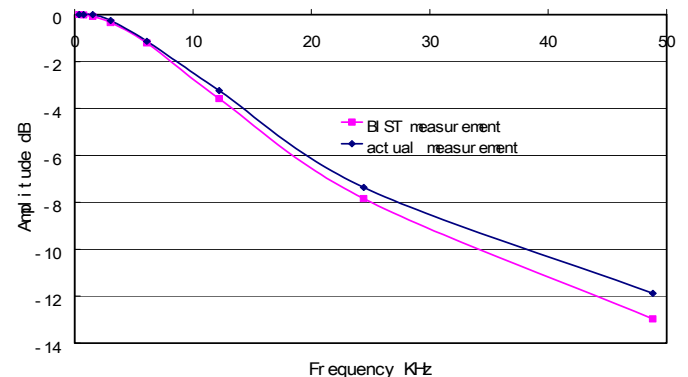


Figure 7. BIST measured amplitude response and actual measurement of 1st order LPF.

The DDS-based TPG, test controller, and multiplier/ accumulator-based ORA were modeled in Verilog along with an interface to allow PC control of the BIST circuitry and retrieval of the BIST results. We synthesized the complete BIST circuit shown in Figure 9, which includes capabilities for measuring linearity and frequency response, into a Xilinx Spartan XC2S50 FPGA. Table I summarizes the synthesis results to give an idea of the area and performance of the complete BIST circuit. The frequency response measurement circuitry shown in Figure 2 uses only a subset of the complete BIST measurement circuit.

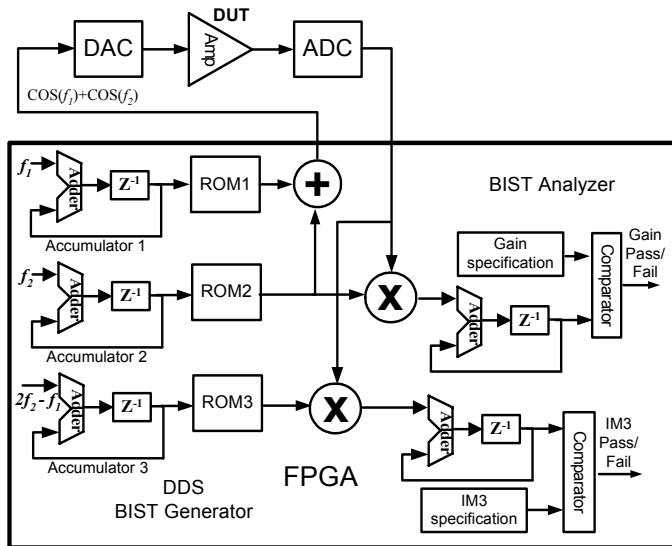


Figure 8. Complete BIST measurement circuit [1].

TABLE I. Synthesis Results for BIST Circuit

FPGA Attribute	Total in FPGA	2-MACC		1-MACC	
		Used by BIST	% Usage	Used by BIST	% Usage
slices	768	313	40%	212	27%
flip-flops	1536	218	14%	158	10%
4-input LUTs	1536	572	37%	390	25%

The synthesis results in Table I are given for two implementations. One implementation includes two multiplier/accumulator (2-MACC) based ORAs, as illustrated in Figure 2 and Figure 9, such that DC_3 and DC_4 are obtained simultaneously during the same BIST sequence. The second implementation includes only one multiplier/accumulator (1-MACC) based ORA with DC_3 and DC_4 obtained during separate but identical BIST sequences. This doubles the test time since the BIST sequence must be executed twice to obtain each DC value, but it reduces the BIST circuitry by a third. In both cases, we use 8-bits of the 12-bit DAC and ADC such that the DDS and multiplier circuits were 8-bits while the accumulators in the ORAs were 16-bits. It should be noted that the XC2S50 is a very small-sized FPGA in the Spartan II series and is the same size as the smallest Virtex I FPGA.

Therefore, the size of the BIST circuitry is quite small with the DDS-based TPG accounting for approximately one-third of the total BIST circuitry.

Our BIST circuitry requires only about 5% of the logic resources that would be needed to implement an FFT-based approach [3]. For example, a 1024-point radix-2 FFT alone requires 3,332 slices in addition to three 18×18 -bit multipliers in a Virtex II or Spartan 3 FPGA [4]. As a result, the FFT circuit alone is more than ten times larger than our complete BIST circuit which also includes the DDS-based TPG, test controller, and PC communications interface. The DAC and ADC are not included in the BIST overhead calculation since the approach is targeted for mixed-signal systems that contain the DAC and ADC as part of the existing design.

V. CONCLUSIONS

We have developed a BIST approach for analog circuit functional testing including measurement of amplifier linearity and frequency response. The DDS-based TPG is used to generate two frequency tones required in the two-tone linearity test as well as single tones for frequency response measurements [1]. The efficient ORA design, consisting of a multiplier and accumulator, avoids using traditional FFT-based spectrum analysis [3], which consumes much more power and die area.

A potential problem identified with the BIST approach is that the ORA suffers from phase delays which distort the gain measurement in frequency response test [2]. This is also a concern during linearity test near the cut-off frequency. In this paper, we have shown that a simple measurement made with a subset of the existing hardware of the BIST approach can determine the actual phase delay. This allows us to not only measure the phase delay of a circuit, but also to correct the measured amplitude for a complete frequency response measurement. In the same manner, the phase delay correction described in this paper can be applied to the linearity measurement described in [1].

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