

Automatic Analog BIST with Pattern Generator and Analyzer

Contact

Brian Wright
Auburn University
Office of Technology Transfer
334-844-4977
brian.wright@auburn.edu
http://ott.auburn.edu/
Reference: DDS BIST

Inventors

Dr. Foster Dai
Associate Professor
Department of Electrical
and Computer Engineering

Dr. Chuck Stroud
Professor
Department of Electrical
and Computer Engineering

References

F. Dai, C. Stroud, D. Yang, and S. Qi, "Automatic Linearity (IP3) Test with Built-in Pattern Generator and Analyzer", *International Test Conference (ITC)*, Charlotte, NC, October, 2004

Status

- Two provisional patent applications have been filed
- The invention has been successfully implemented and verified in hardware using field programmable gate arrays (FPGAs) at Auburn University

Overview

Auburn University seeks a licensee or development partner for an inexpensive built-in self test (BIST) technique for radio frequency integrated circuits (RFICs). This invention could, for the first time, make complete testing of RFIC chips economically feasible.

Advantages

- Eliminates the need for expensive analog test equipment for RFICs
- Enables complete testing of RFIC chips
- Generates precise frequency tones for analog tests
- Enables accurate phase delay measurement
- Occupies much less area on the chip compared to existing solutions
- Generates more waveforms for tests than competing DDS techniques
- Compensates for temperature, voltage and other fluctuations

Description

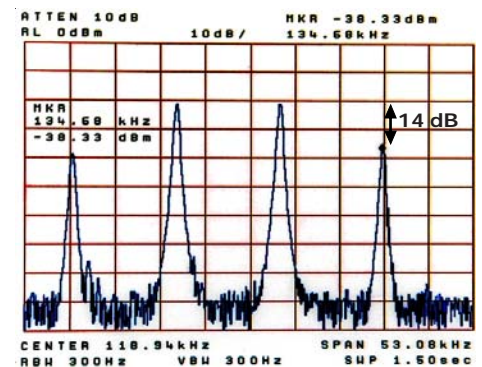
The current manual analog testing process for high-speed RFICs is time consuming and costly, rising to as much as 50 percent of the manufacturing cost due to costly test equipment, cumbersome test preparation and the lack of a standardized methodology. As a result, only a small sample of RF circuitry is currently tested.

RFIC testing is sensitive to supply voltage and process variations which makes external testing difficult. Our BIST technique provides analog test capability as well as an efficient technique for calibrating and compensating analog circuitry that is sensitive to temperature, supply voltage and process variations. Existing techniques cannot perform complete tests such as frequency response or noise and modulation, and in some cases require much more chip area overhead than Auburn's method and are not precise enough for analog tests such as analog modulation.

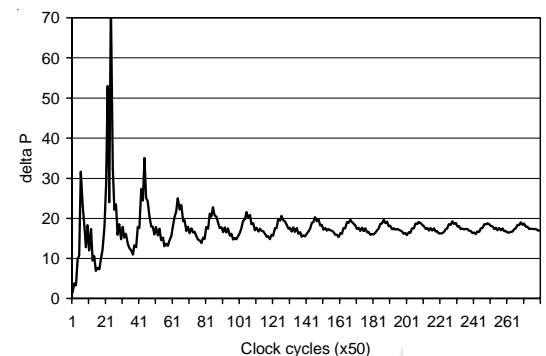
Dr. Stroud's and Dr. Dai's invention is a DDS-based BIST approach that generates various modulated waveforms for analog functionality tests. This BIST approach consists of a test pattern generator (TPG) and an output result analyzer (ORA). The TPG can provide precise frequency tones for many analog tests and can implement various waveforms such as chirp, ramp, MSK, QAM and other hybrid modulations. Our BIST circuitry has the ability to provide accurate phase information that can be used to tune other functional measurements (such as linearity and gain) for better fault detection. Tests of Auburn's BIST technique show extreme consistency of the output. (In 1000 BIST measurements of an actual ΔP of 14.3dB, BIST output was 14.3, and variance was 0.00003.) None of the existing analog testing schemes compare favorably with the comprehensive modulated waveform generation of Auburn's DDS synthesizer, which for the first time could make complete testing of RFICs economically feasible.

Licensing Opportunities

- This technology is available for exclusive or non-exclusive licensing
- Joint development opportunities include funded research or a joint venture



Spectrum analyzer measurement of two-tone test at the amplifier output showing $\Delta P = 14$ dB.



ΔP value vs. clock samples measured by BIST hardware indicating 14 dB.