

BUILT-IN SELF-TEST AND DIAGNOSIS OF MULTIPLE EMBEDDED CORES IN SoCs

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ABSTRACT: A new approach is presented for Built-In Self-Test (BIST) and diagnosis of embedded cores in System-on-Chip (SoC) devices using an embedded Field Programmable Gate Array (FPGA) core. The approach targets multiple regular structure cores including memories, multipliers, etc., but can be used to test any set of multiple identical cores in a SoC that also contains an embedded FPGA core with access to the cores to be tested. The approach can be used for manufacturing testing or in-system test and diagnosis for fault-tolerant applications. Experimental results are presented from the actual implementation of the BIST and diagnostic approach in commercial configurable SoCs and FPGAs that contain multiple regular structure cores.