

# **Delay Detection in the Slack Interval: A new delay test methodology**

**Haihua Yan and Adit D. Singh**

**Department of Electrical & Computer  
Engineering**

**Auburn University, AL 36849**

# Introduction

## How well must we test?

### Approximate order-of-magnitude estimation

- Number of parts per typical system: 100
- Acceptable system defect rate: 1% (1 per 100)
- Therefore, required part reliability

1 defect in 10,000

100 Defects Per Million

100 DPM

Desired ~100 DPM for commercial ICs (ideal)

~1000 DPM acceptable for some ASICs

# How well must we test?

**Assume 2 million ICs manufactured with 50% yield**

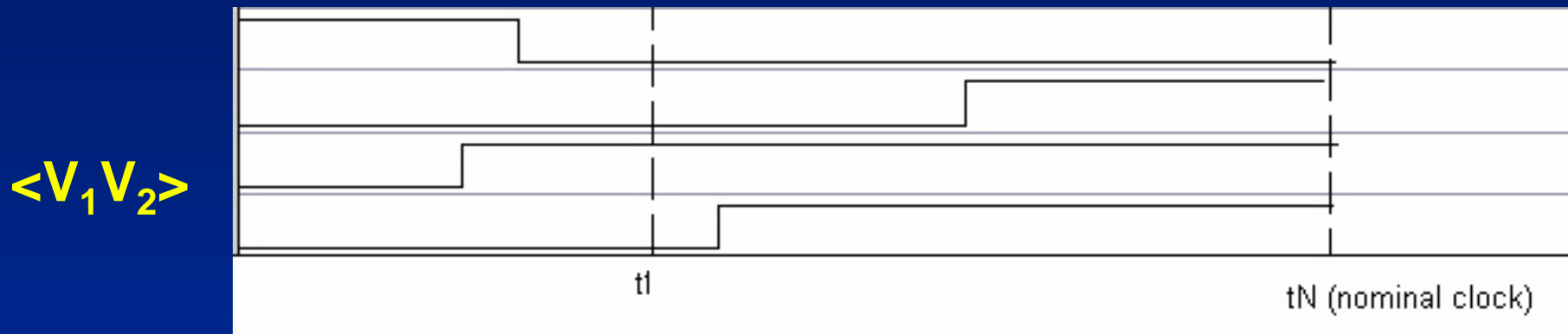
- 1 million GOOD >> shipped
- 1 million BAD >> test escapes cause defective parts to be shipped

For 100 BAD parts in 1M shipped (DPM=100)

Test must detect 999,900 out of the 1,000,000 BAD

For 100 DPM: Needed Test Coverage = 99.99%

# Timing Tests



$V_1$      $V_2$

- Two sequential test vector inputs  $\langle V_1 V_2 \rangle$  cause a change at an output
- The switching delay is the time from the application (launch) of  $V_2$  until change at the output

# Scan Based Delay Testing

# Launch-on-Shift

## LOGIC

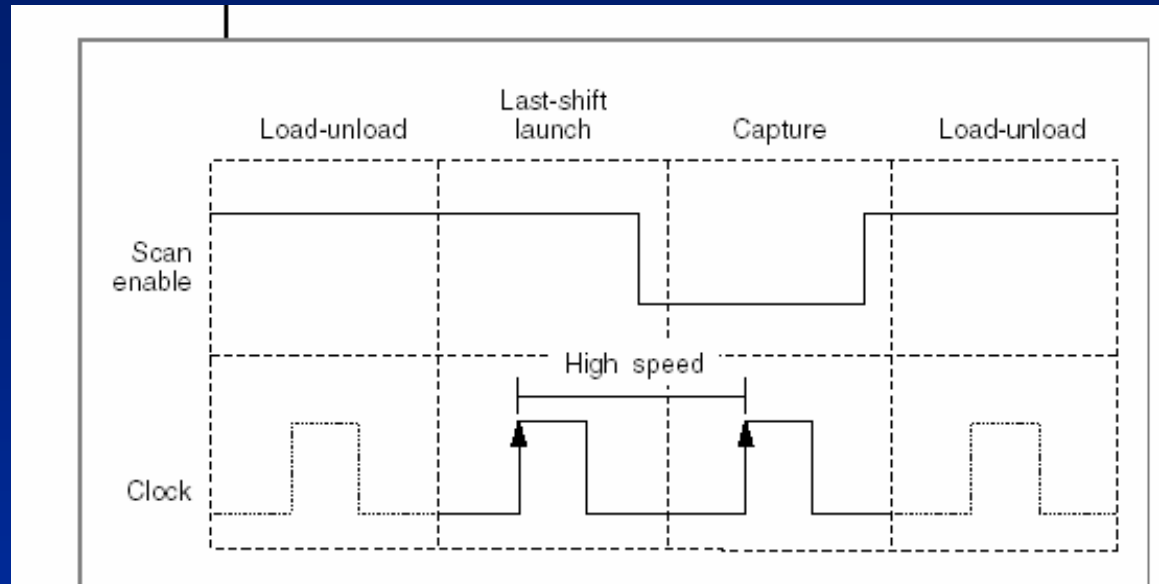
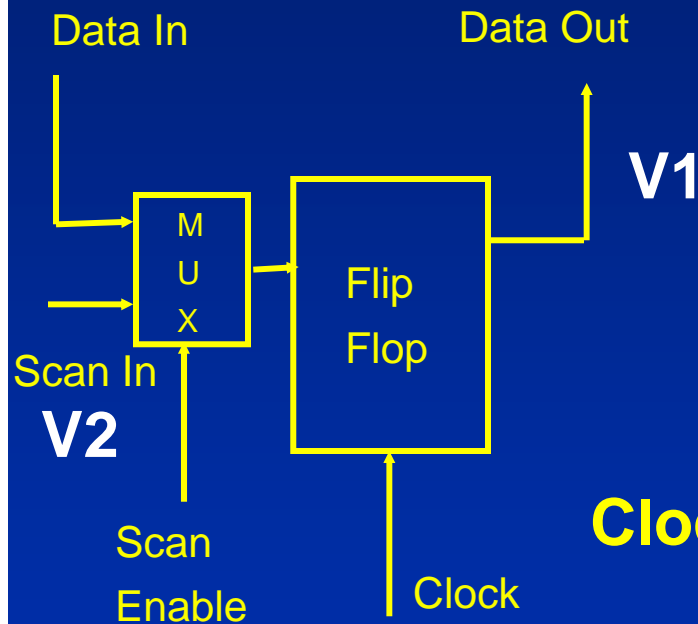


Figure 3. A simplified timing diagram of a launch-from-shift transition delay fault (TDF) pattern.

**Clock Edge 1: Launch V2 (scan = 1)**

**Then switch scan = 0**

**Clock Edge 2: Capture response to V1 > V2 change in Flip Flop**

# Scan Based Delay Testing

## Launch-on-Capture

### LOGIC

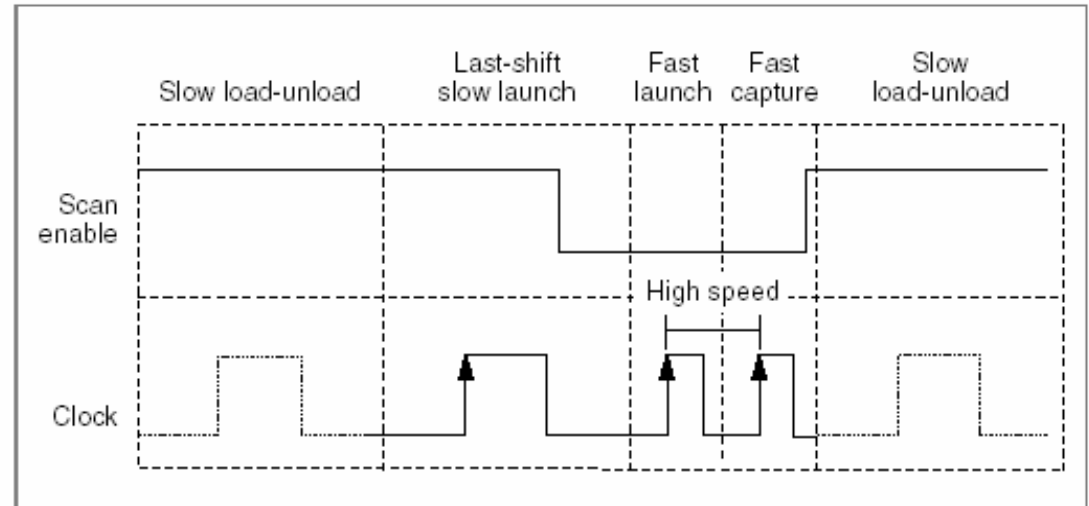
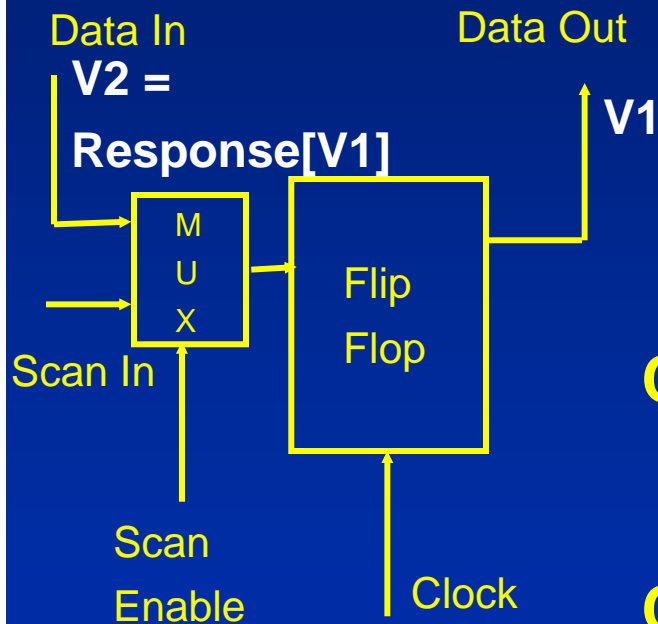


Figure 4. Simplified timing diagram of a launch-from-capture (broadside) TDF pattern.

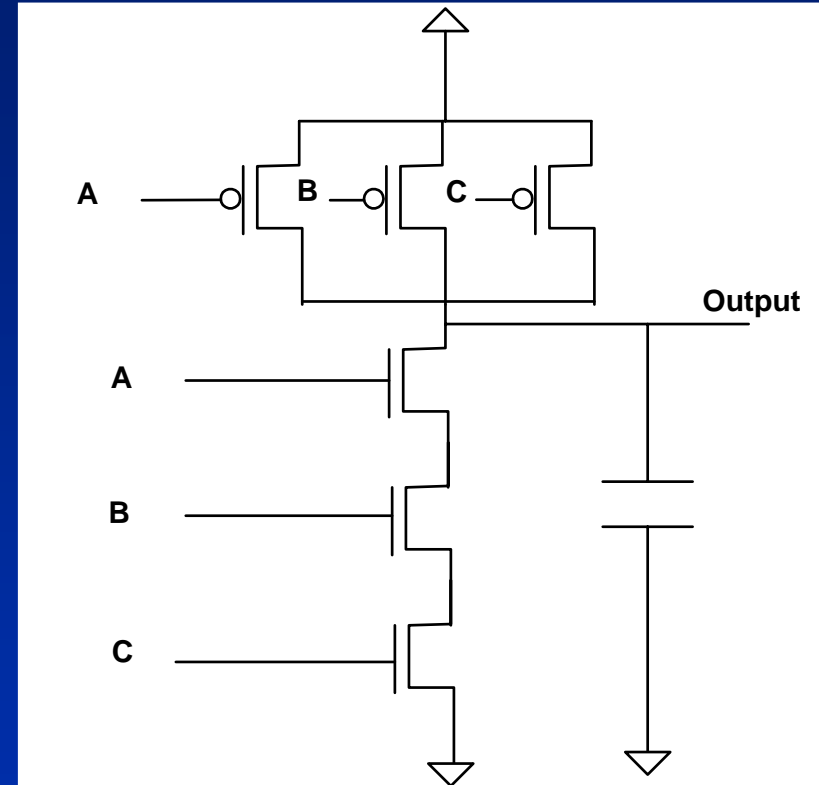
**Clock Edge 1: Apply V1 (scan = 1)  
Then switch scan = 0**

**Clock Edge 2: Capture response to V1 in  
Flip Flop to launch timed  
transition. This is V2**

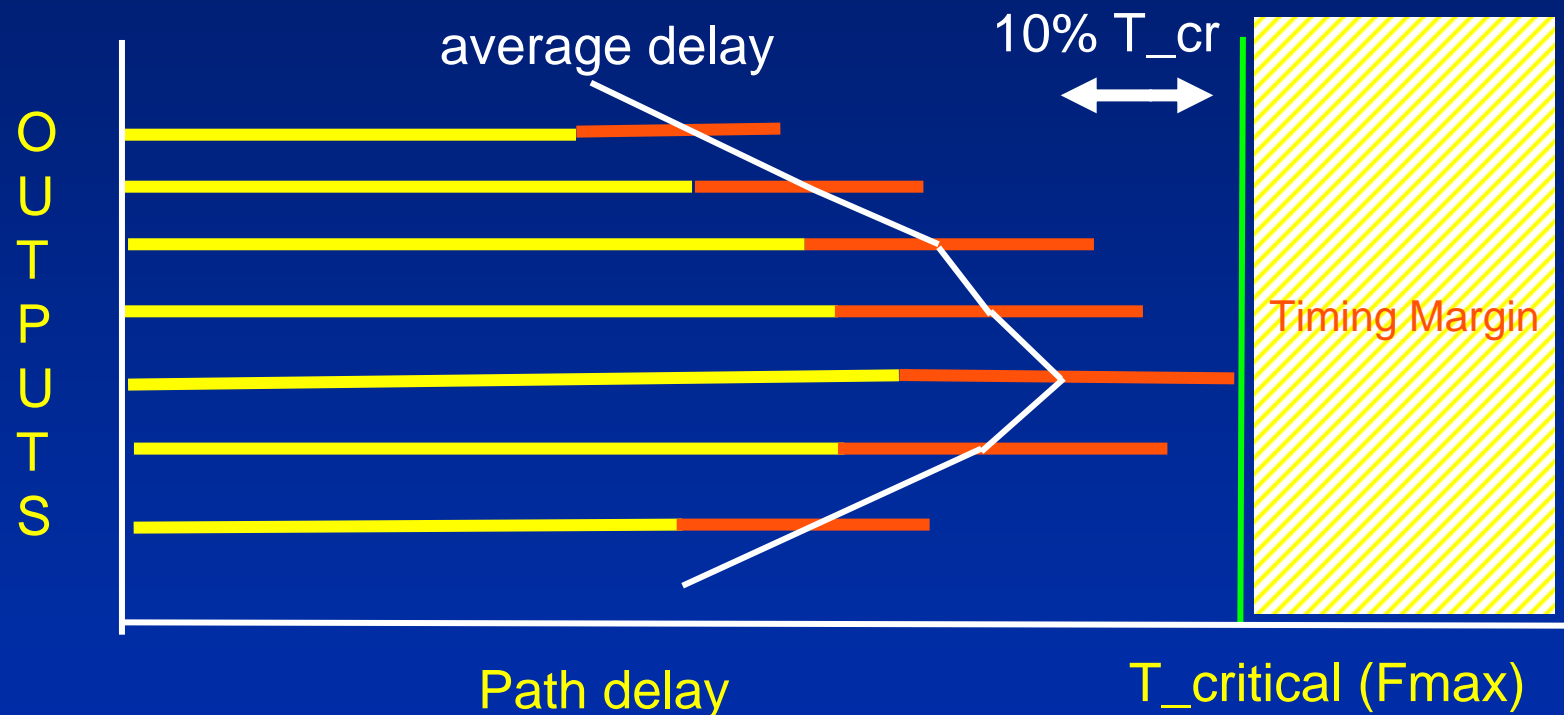
**Clock Edge 3: Capture response to V2**

# Variations in CMOS Delays

- Switching delays in CMOS greatly depend on the off path signals and internal circuit state
- Hard to find  $\langle V_1 V_2 \rangle$  to ensure worst case conditions for signal propagation along a path.
- Often this worst case test vector pair can be different for the same circuit depending on fabrication parameters



# Input based variations in path delays for CMOS Logic



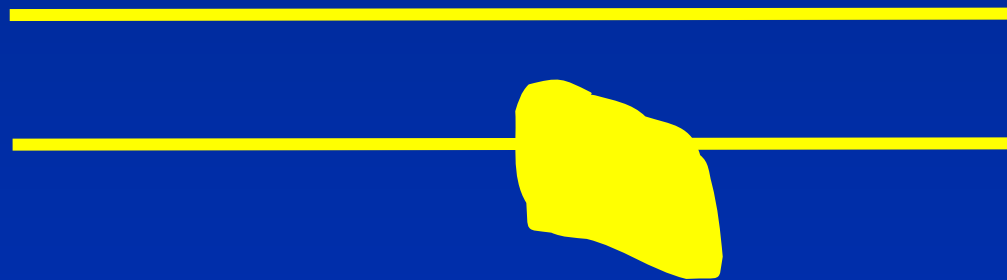
Defects that increase path delay by less than 10% of  $T_{critical}$  are virtually undetectable even with  $F_{max}$  testing

# The Problem of Latent Defects

## Killer Defect



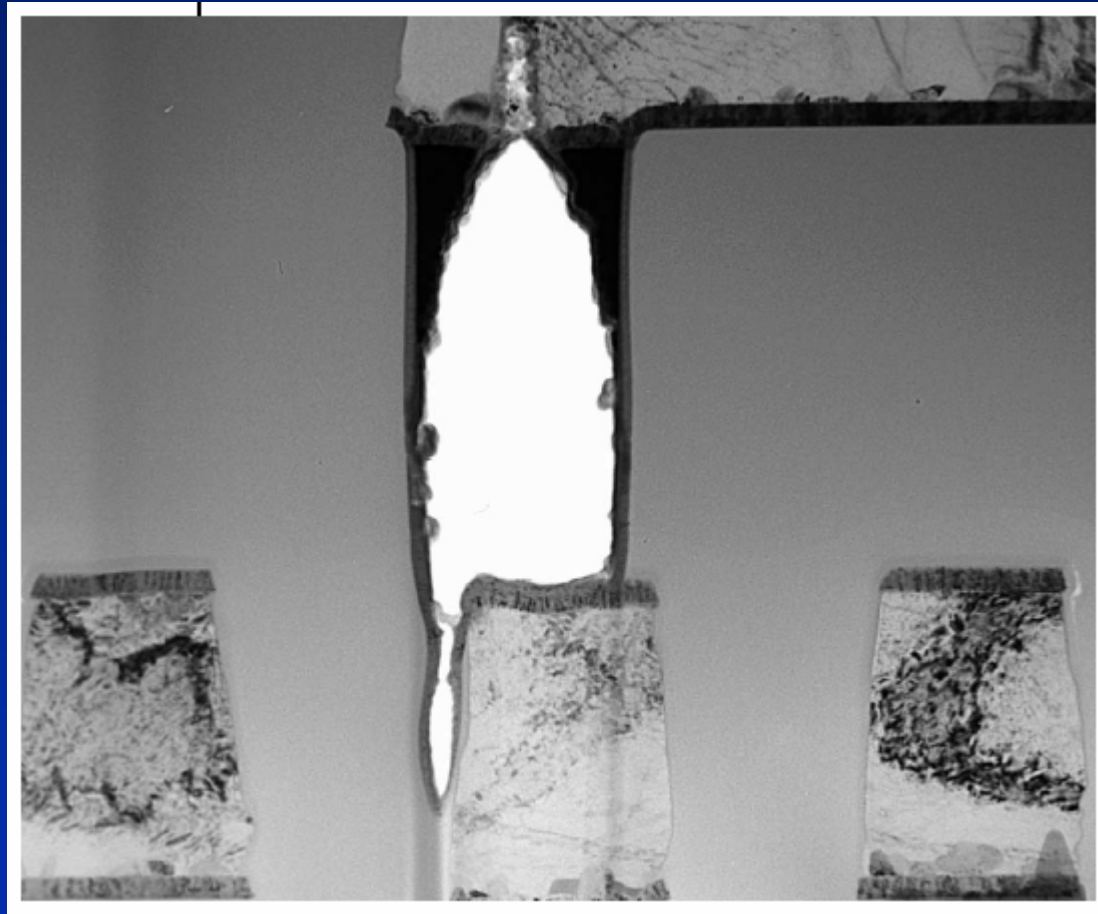
-Detected at  
wafer probe



-Must be stress  
tested, or  
screened  
(statistically)

## Latent Defect

# Resistive Via



**Resistive open due to unfilled via causing a TDF. The white area is a void that should be filled with tungsten [6].**

# The Problem of Latent Defects

- Between 1% and 0.1% of circuits that pass wafer probe testing have latent defects
  - >> 10,000 to 1000 DPM
- Screened by expensive Burn-in tests
- All microprocessors are burned in
- Burn-in is too expensive for ASICs
- Other test screens are desired

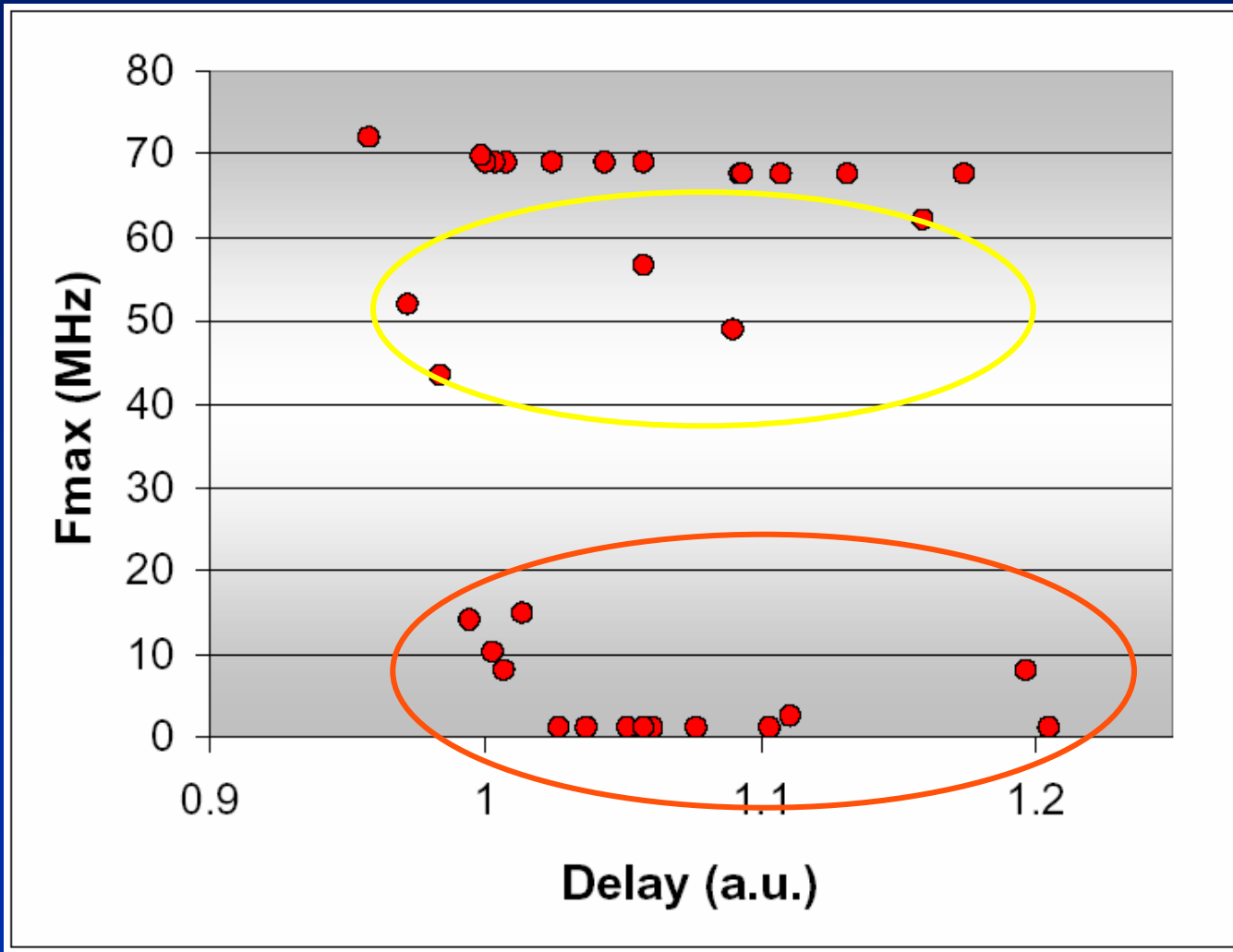
# Latent Defects Screening Tests

- IDDQ Testing can screen latent faults but is losing effectiveness
- LSI Logic uses Fmax testing as a test screen for latent faults
- Fmax testing finds the fastest clock rate at which the circuit under test will still pass a scan based Transition Delay Fault (TDF) test

# Fmax Testing

- Fmax Testing finds the highest clock rate for which a circuit passes a given (TDF) test set
- A binary search using repeated applications of the test set is performed to obtain Fmax
- An abnormal Fmax value compared to other circuits from the lot indicates a defect that may cause a functional or reliability failure in the field

# Fmax Testing

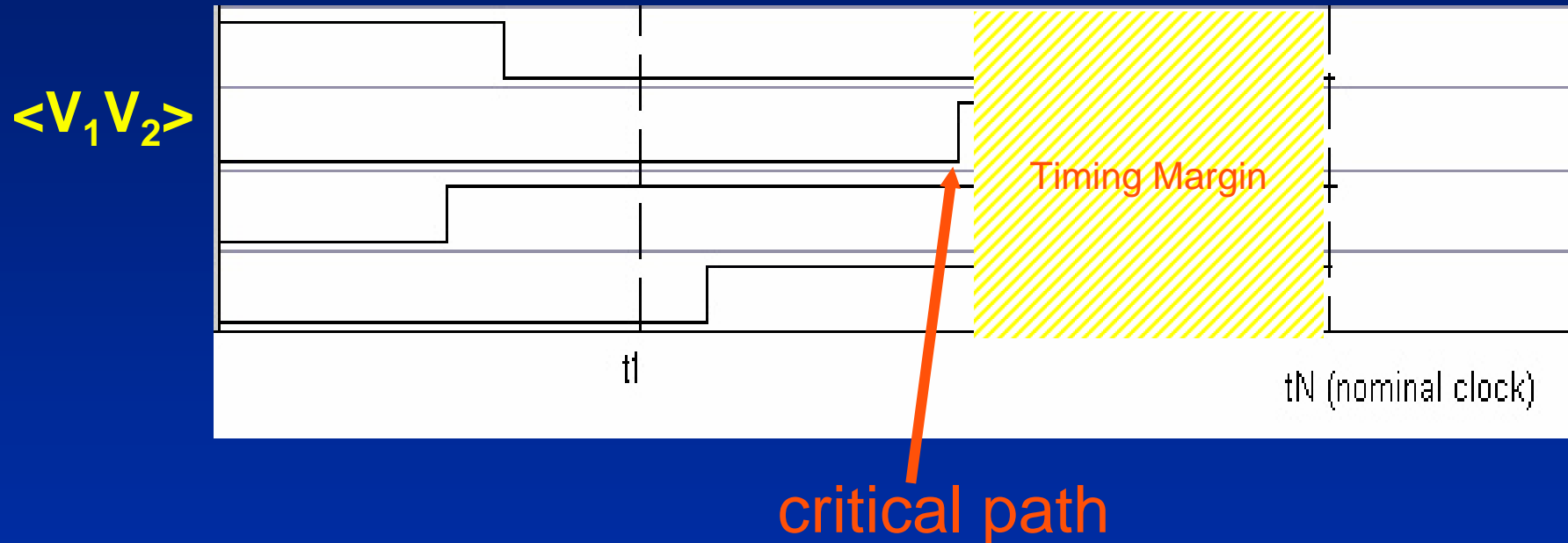


← Intrinsic Clock

← Operational Clock

**Fmax for TDF pattern for 32 parts that pass dc tests but fail system level tests [1]**

# Fmax Testing can observe delays defects in the Timing Margin



- Timing margins to allow for parameter variations, clock skew, variations in test conditions.

# Fmax Testing

- Fmax outliers may experience a delay failure in the field because delay test sets often cannot test worst case signal propagation conditions
- Fmax outliers may also contain latent defects that can cause early life failure

# Latent Defect Screening using Fmax Testing

- Unfortunately, Fmax testing is found to only reduce latent defects by about 30-50%
- The problem:
  - poor delay coverage of the test set. It is very difficult to find good two-pattern tests that propagate worst case delays through circuits
  - Many delays due to defects are absorbed by timing slacks and not observed at the output

# ISCAS 89 Timing Simulation Results For Scan based TDF (Launch-on-shift)

ISCAS89 Full Scan	Size of Fault List	Delay Fault Size (% of $T_{critical}$ )	Traditional Delay Test Coverage		Transition Test Coverage
			fmax	10% Timing margin	
S13207.1	26414	15%	3.08%	1.03%	89.9%
		25%	15.40%	3.61%	
S15850.1	31700	15%	6.94%	0.52%	94.8%
		25%	21.87%	6.77%	
S35932	71864	15%	1.07%	1.05%	86.7%
		25%	12.63%	1.14%	
S38584.1	77168	15%	1.36%	1.08%	88.8%
		25%	9.30%	1.44%	
S38417	76834	15%	1.24%	0.13%	93.6%
		25%	5.98%	1.40%	

# Are these “small” defects worth detecting?

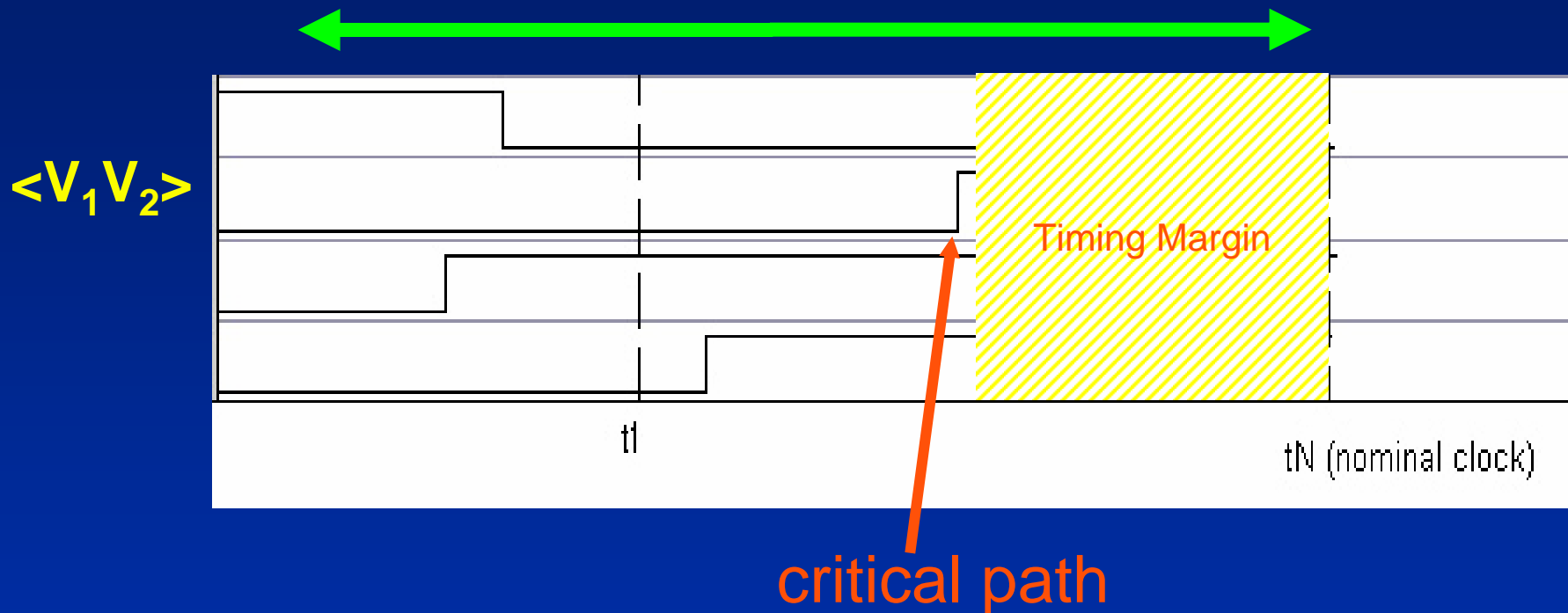
- Are they significant defects?

- For a 8 level critical path, average gate delay is 12.5% of  $T_{critical}$
- 25% extra path delay implies a 200% increase in the delay for some gate - significant!
  - e.g. Via resistance must grow 1,000-10,000X from 0.1ohm (typical) to cause such a delay

# DDSI: Delay Detection in the Slack Interval

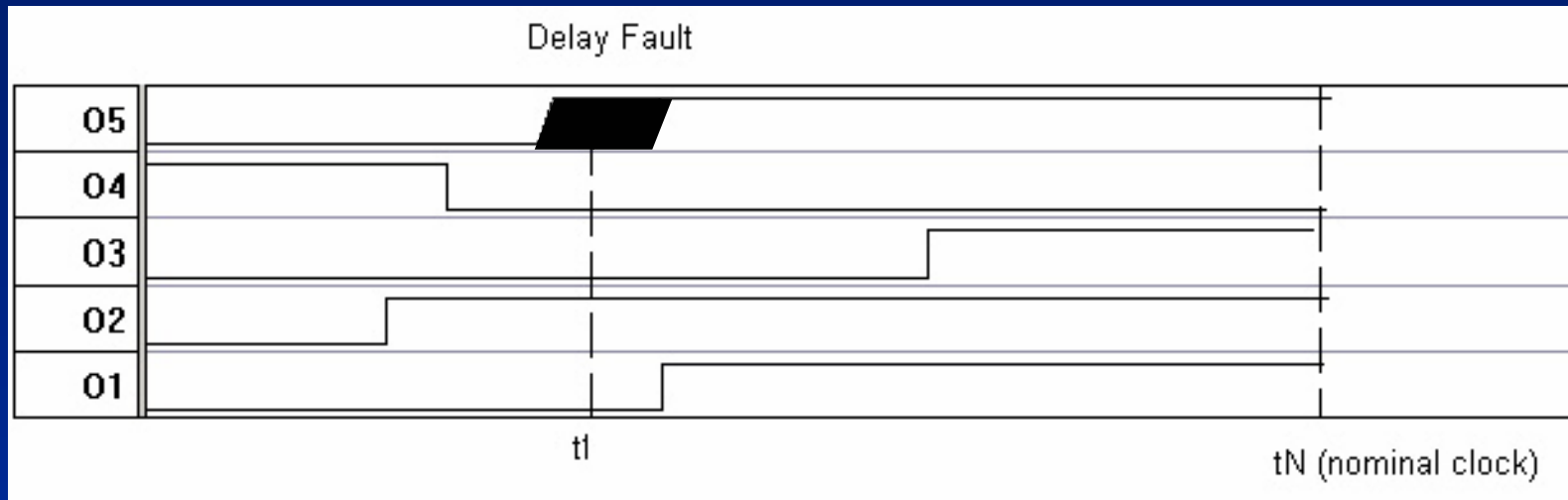
- Like Fmax and minVDD testing, DDSI detects delays caused by random defects or circuit timing anomalies
- Abnormal delay are identified by comparing timing of CUT response to that for identical signals in matched neighboring die.
- Timing anomalies are detected beyond the normal clock period not just until  $T_{critical}$ , but ***also in the slack interval***

# DDSI observes delays defects in the Slack Interval



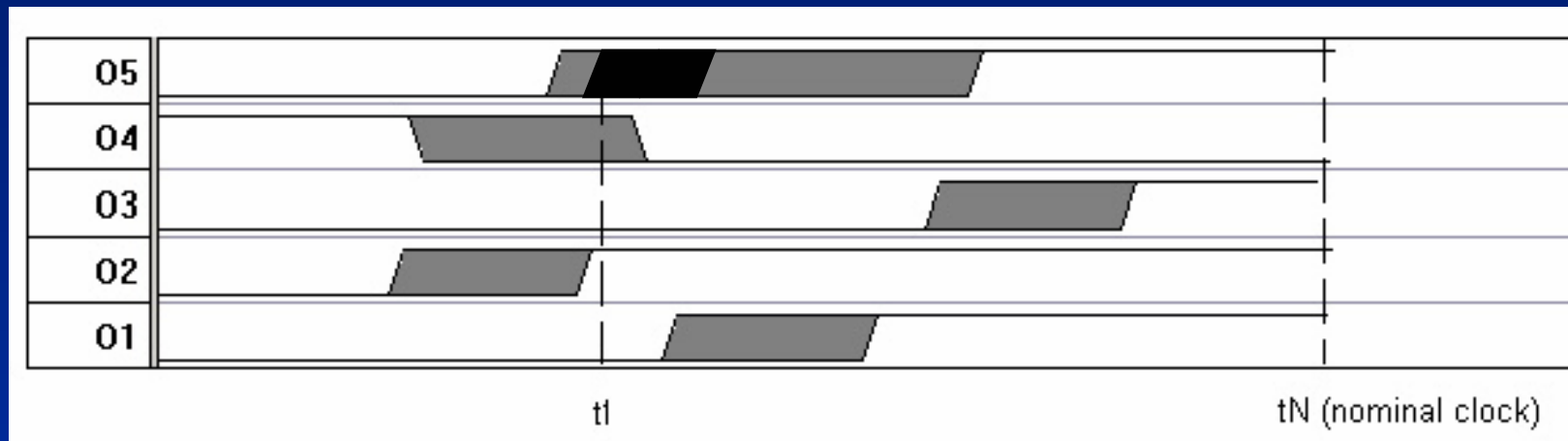
- Delay anomalies beyond the typical 3-5% inter die timing variation due to parameter variations can be reliably detected

# Switching Waveforms in a Clock Period



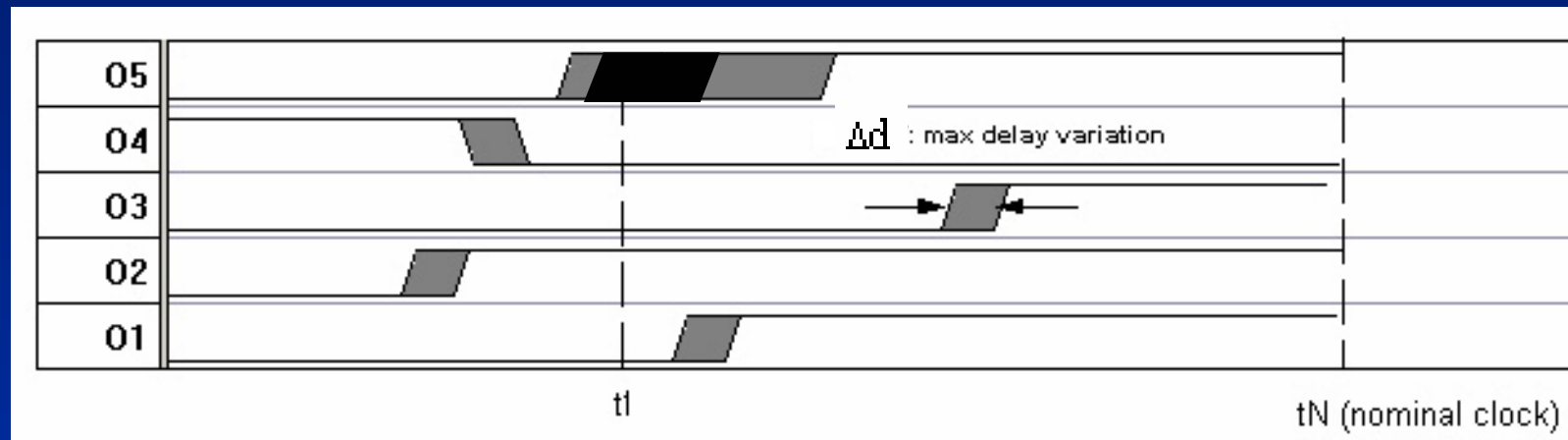
- Delay fault not detected if the output is observed at nominal clock time.
- Delay fault can be “potentially” detected if observed at  $t_1$  ( $t_1 < t_N$ )

# Switching Delay Variations due to Process Parameters



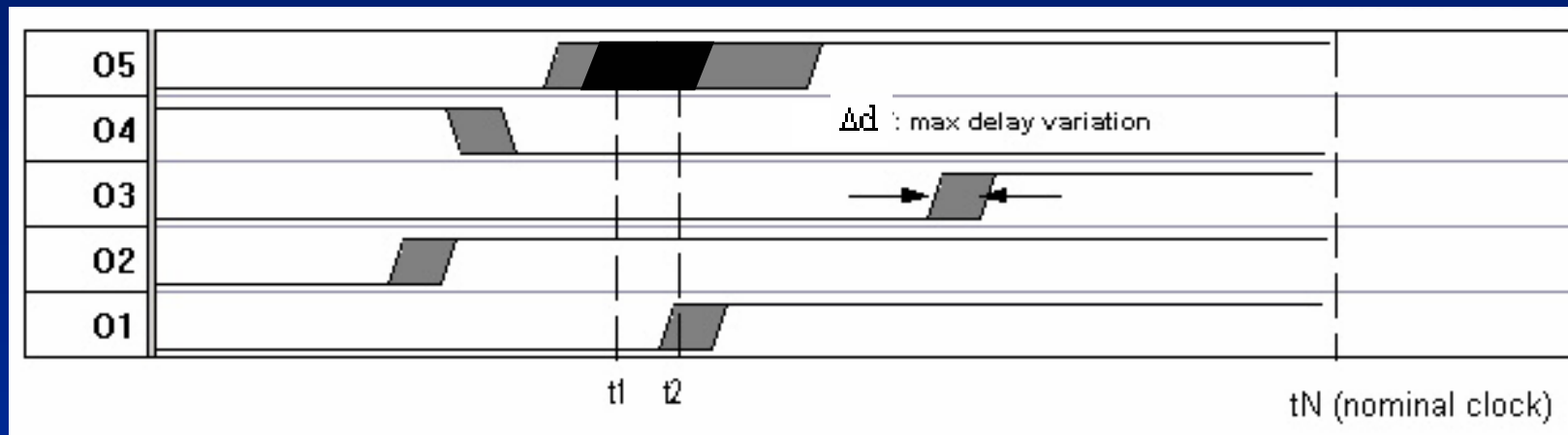
- In practice, delay fault cannot be detected by observing output at  $t_1$  because of normal process parameter variation.
- Expected “good” response at  $t_1$  cannot be reliably known to verify correct output response of the DUT.

# Switching Delay Variation between Adjacent Dies



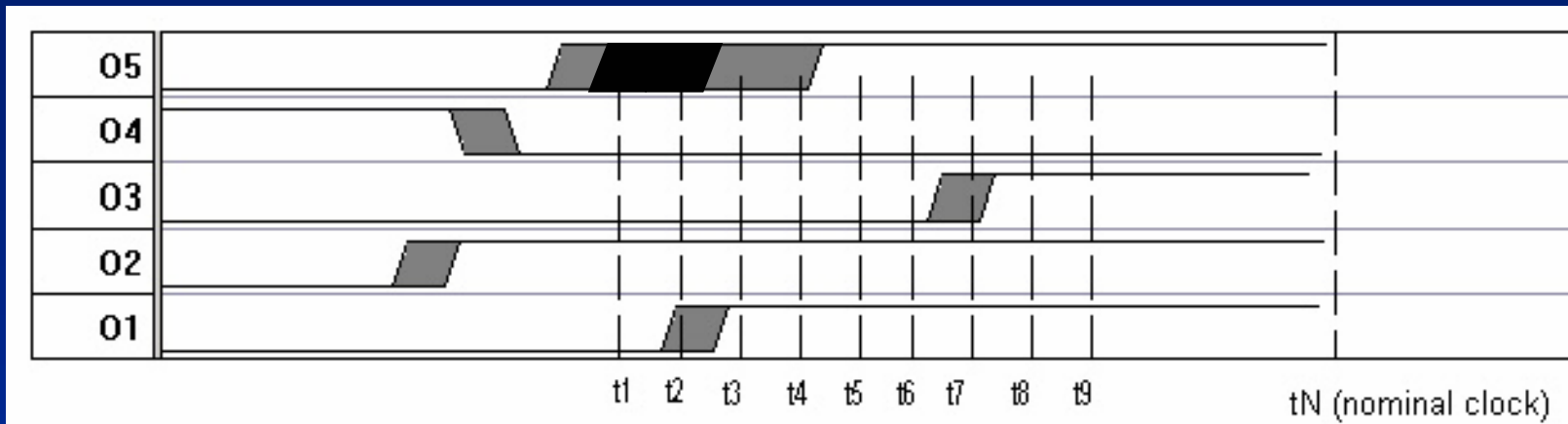
- Because manufacturing parameters track, delay variation between adjacent die on any wafer is much less than that for the entire production.
- Experiments indicate that  $\Delta d$  is 2~3%; usually less than 5%.

# Detecting Delay Faults



- Delay defect can be detected if a signal in the DUT has still not switched at time  $t_2$  ( $t_2 - t_1 > \Delta d$ ) when a known good neighbor switches at  $t_1$ .

# Detecting Delay Faults Using Multiple Fast Clocks



- Output captured at multiple  $\Delta t$  time intervals ( $t_N - t_{N-1} = \Delta t$ )
- **Delay fault** if signal switches in a good neighbor at time  $t_N$  and has still not switched in the DUT at time  $t_N + \Delta d + \Delta t$ ; i.e. the first sampling point that allows for a  $\Delta d$  switching variation

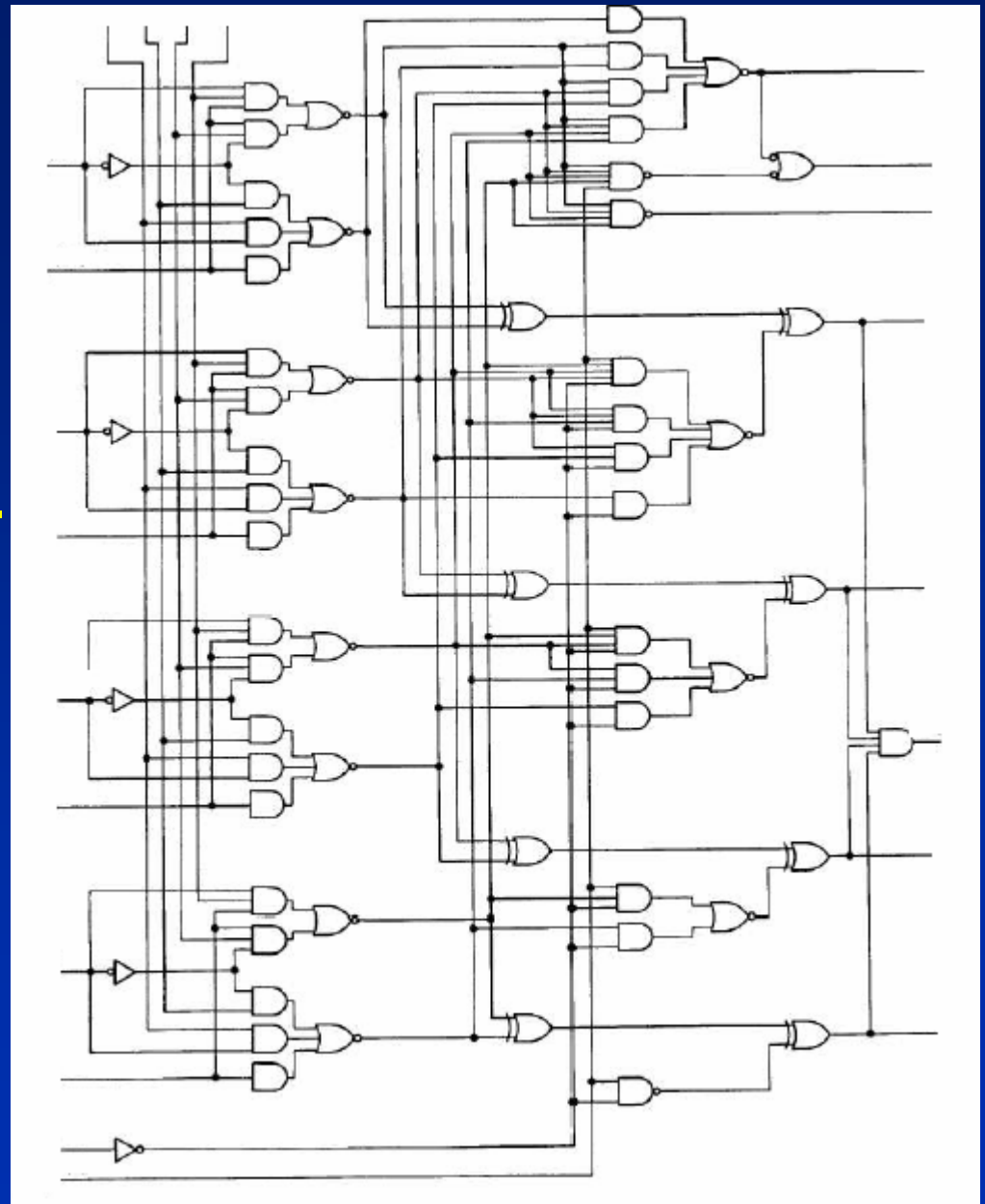
# Test Chip Design

## Test Chip construction:

- Experimental datapath chip was designed and fabricated through MOSIS using AMI5 (0.5 micron) technology.
- IMS Tester was used to detect the injected delay faults. (0.1 ns maximum timing resolution for clock control)

# Test Circuit

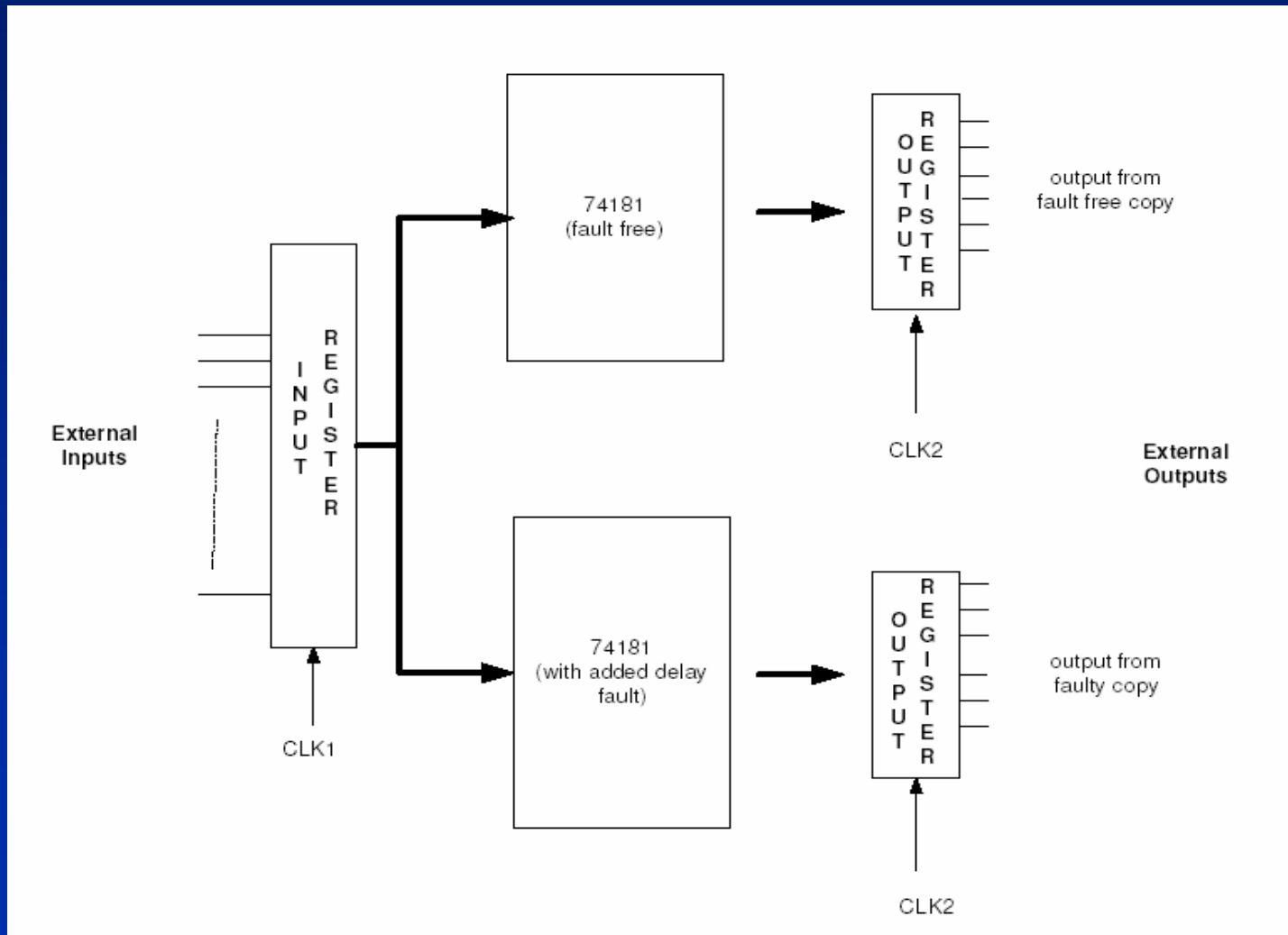
- An ALU circuit, 74181 was used. Combinational circuit with 14 inputs and 8 outputs.



# Test Chip Structure

- Two copies of 74181 were placed in the same die to ensure they are physical neighbors.
- Delays were introduced in (3 of 8) outputs of one of the circuits by adding extra capacitive loading on some gate outputs
- The layouts were kept identical except for the modifications to introduce the “delay faults”

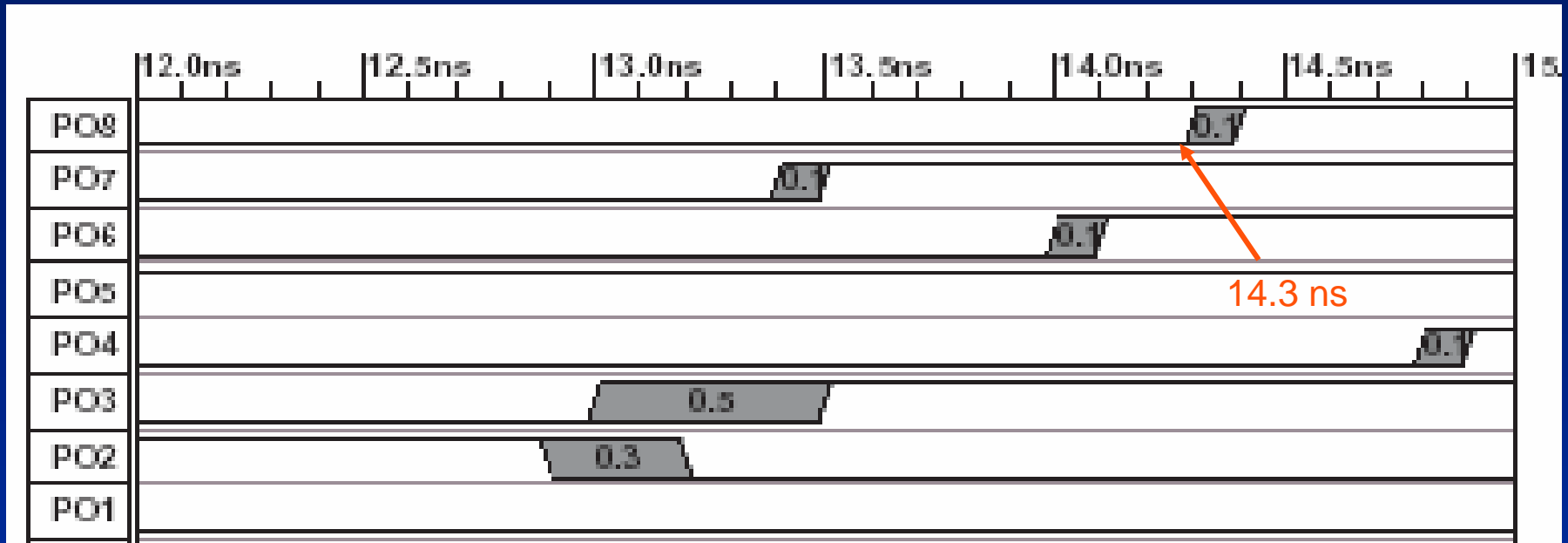
# Test Chip Layout



# Test Procedure

- $\langle v1, v2 \rangle$  test vector pairs were applied
- Output transitions were recorded at multiple times in increment of 0.1 ns

# Test Procedure

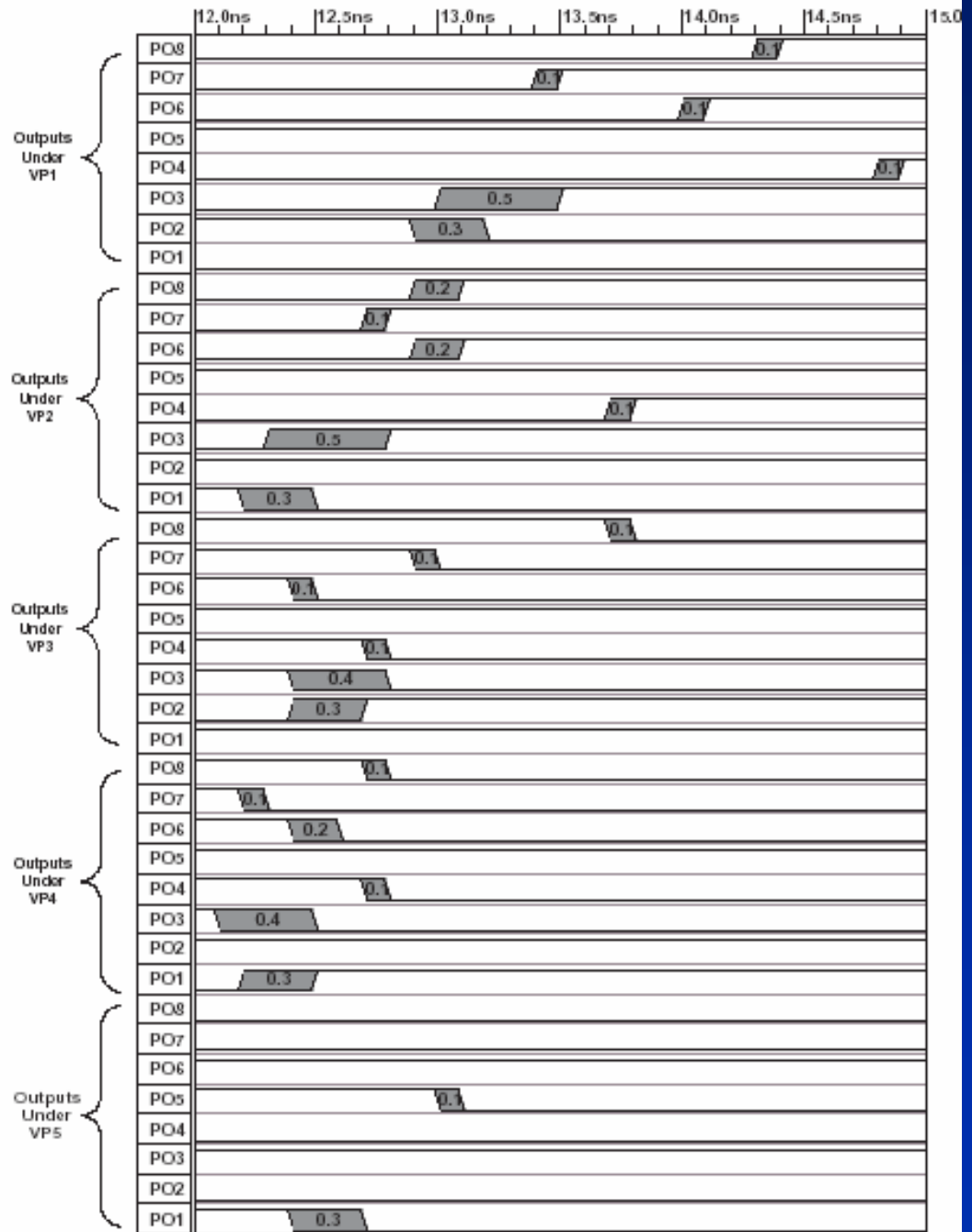


- In tabulating switching delays, a signal is assigned a switching delay of  $t_n$  if it is observed to switch during the 0.1ns interval between  $t_n$  and  $t_{n+1}$ .
- The *switching window* for the two transitions (transitions from faulty and fault-free copies of circuits.) for the  $\langle v1, v2 \rangle$  vector pair is computed to be the maximum possible switching delay variation between the two copies of circuits.

# Test Results for Chip#1

**PO 1-3 Faulty**

**PO 4-8 Failure Free**

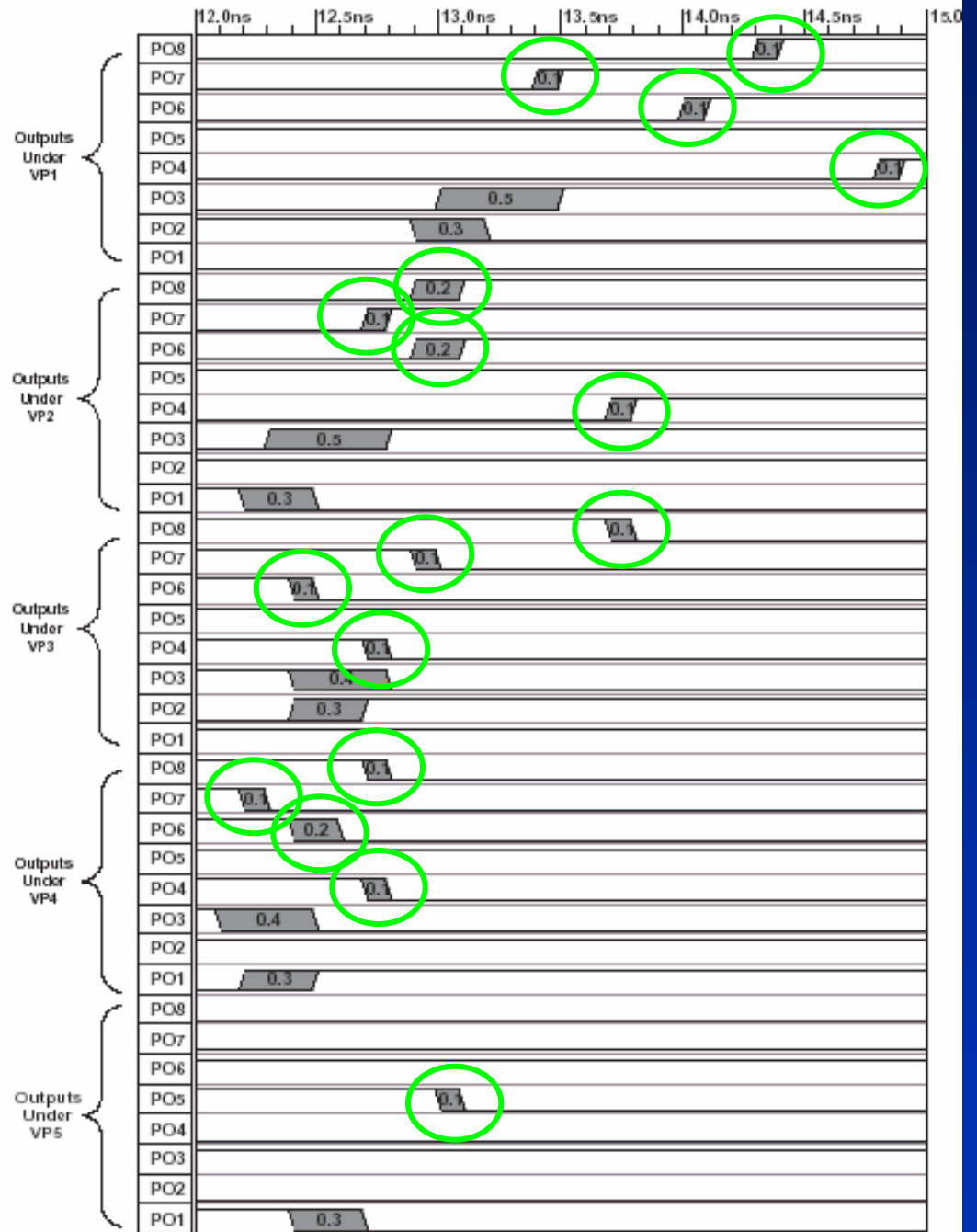


(a) Output transitions of experimental chip1 for five test vector pairs

# Test Results for Chip#1

PO 1-3 Faulty

PO 4-8 Failure Free

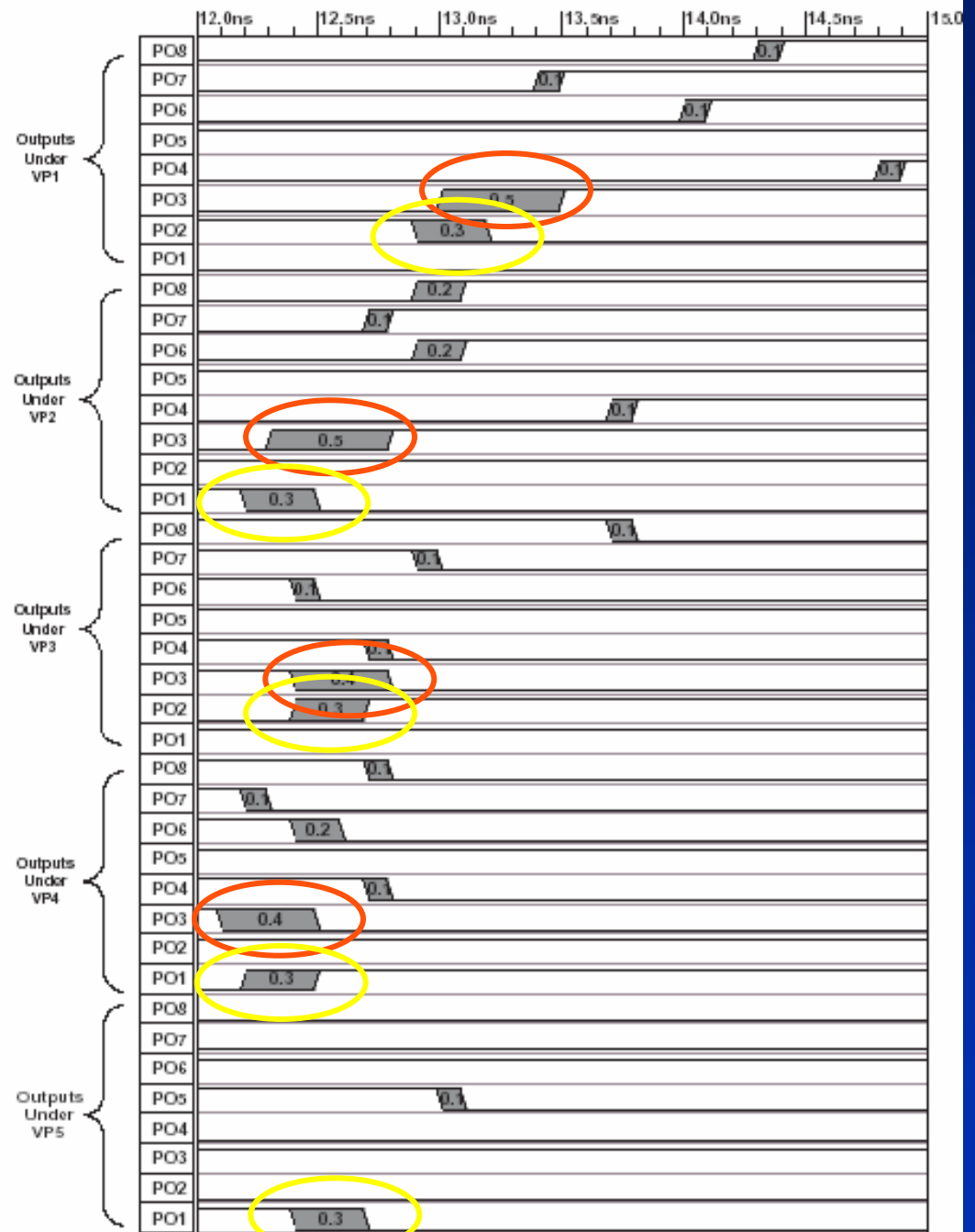


(a) Output transitions of experimental chip1 for five test vector pairs

# Test Results for Chip#1

**PO 1-3 Faulty**

**PO 4-8 Failure Free**



(a) Output transitions of experimental chip1 for five test vector pairs

# Test Results for Chip#5

- Five packaged test chips were returned by MOSIS
- The results for 3 of the other 4 chips were very similar
- However, Chip#5 displayed an unusual response

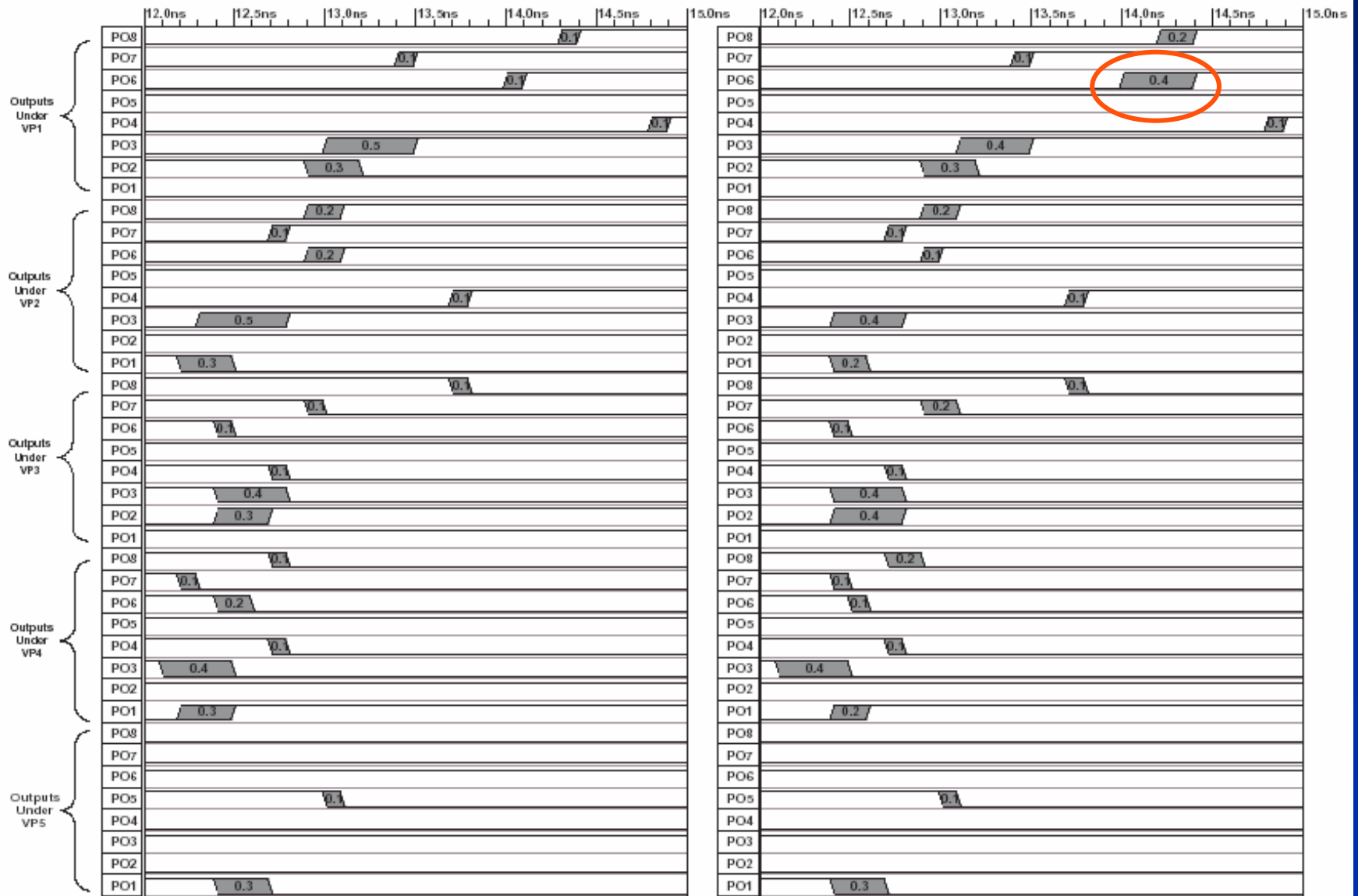
# Test Results for Chip#5



(a) Output transitions of experimental chip1 for five test vector pairs

(b) Output transitions of experimental chip5 for the same five test vector pairs

# Test Results for Chip#5



(a) Output transitions of experimental chip1 for five test vector pairs

(b) Output transitions of experimental chip5 for the same five test vector pairs

# Investigation of the “Real” Fabrication Delay Fault

- Packaged chips received from MOSIS cannot be guaranteed to be strict neighbors, but can be expected to be physically close on the same wafer.
- The “real” delay fault was studied by comparing switching delays at this output (for the fault free circuits) among the 5 copies fabricated

# Investigation of the Real Fabrication Delay Fault

SWITCHING WINDOWS FOR TRANSITIONS AT FIVE CHIPS

<i>Chip#</i>	PO7		PO8		PO6	
	0 → 1	1 → 0	0 → 1	1 → 0	0 → 1	1 → 0
1	13.0	12.4	14.9	12.9	12.4	12.9
2	13.1	12.4	14.9	12.9	12.4	12.9
3	13.0	12.5	15.0	13.0	12.5	12.9
4	13.0	12.5	14.9	13.1	12.4	12.9
$\Delta W(1 - 4)$	0.2	0.2	0.2	0.3	0.2	0.1
5	13.5	12.5	15.3	13.0	12.4	13.3
$\Delta W(1 - 5)$	0.6	0.2	0.5	0.3	0.2	0.5

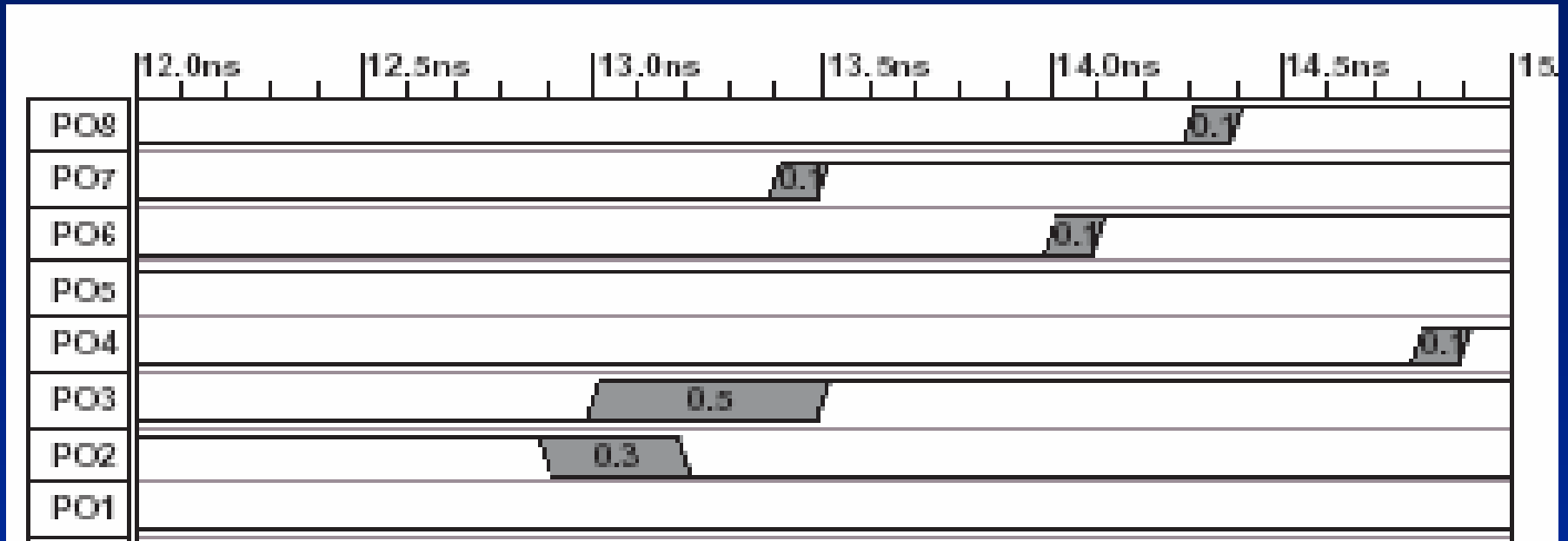
$\Delta W(1 - 4)$ : switching window for Chip#1-4

$\Delta W(1 - 5)$ : switching window for Chip#1-5

# Discussion

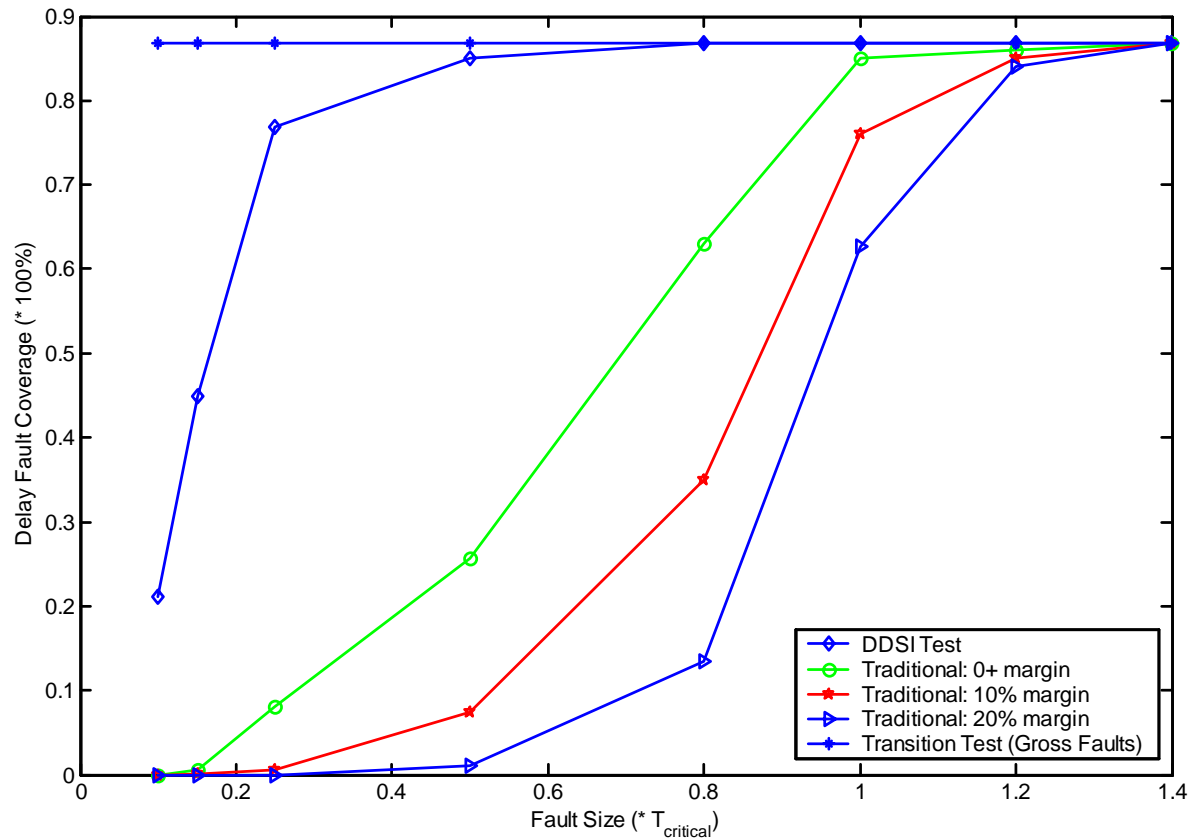
- For chips 1-4 switching delays were still matched, with the switching window ranging from 0.1-0.3 ns.
- The test detected a real delay of  $\sim 0.5\text{ns}$  or 4% of the path delay.

# Discussion



- Recall traditional tests require the extra delay to be observed at the nominal clock time.
- Because of timing margins to allow for parameter variations among good circuits in the production lot, it is virtually impossible to detect delays  $<10\%$  of path delay
- A 10% path delay increase can reflect a 50-100% increase in delay for some gate –a significant defect that can be a reliability risk

# Detection of Relatively Small Delay Faults



Simulation results for S38584.1

# Full-scan ISCAS 89 Simulation (Launch-on-shift)

ISCAS89 Full Scan	Size of Fault List/ Size of Test Set	Delay Fault Size (% of $T_{critical}$ )	DDSI Test Coverage	Traditional Delay Test Coverage		Transition Test Coverage
				0+% Timing margin	10% Timing margin	
S13207.1	26414/635	10%	45.7%	0.2%	0	85.1%
		15%	53.3%	2.8%	0.3%	
		25%	76.0%	14.3%	2.6%	
S15850.1	31700/453	10%	43.9%	0	0	92.5%
		15%	56.3%	6.7%	0.1%	
		25%	68.5%	21.2%	6.5%	
S35932	71864/66	10%	25.2%	0.1%	0	84.5%
		15%	41.3%	0.9%	0.1%	
		25%	54.7%	12.6%	1%	
S38584.1	77168/190	10%	20.4%	0	0	86.8%
		15%	43.2%	0.5%	0.1%	
		25%	73.6%	8.1%	0.5%	
S38417	76834/353	10%	37.1%	0	0	91.4%
		15%	54.6%	0.2%	0	
		25%	70.4%	5.4%	0.2%	

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S38417	76834/353	10%	37.1%	0	0	91.4%
		15%	54.6%	0.2%	0	
		25%	70.4%	5.4%	0.2%	

# Conclusion

- Experimental results show good potential for detecting many of the delay faults missed by traditional scan based delay tests
- May be possible to achieve high quality testing using scan based methods alone
- Such tests can be supported by slow low cost testers