

# Multi-Mode Scan: Test-per-Clock BIST for IP Cores

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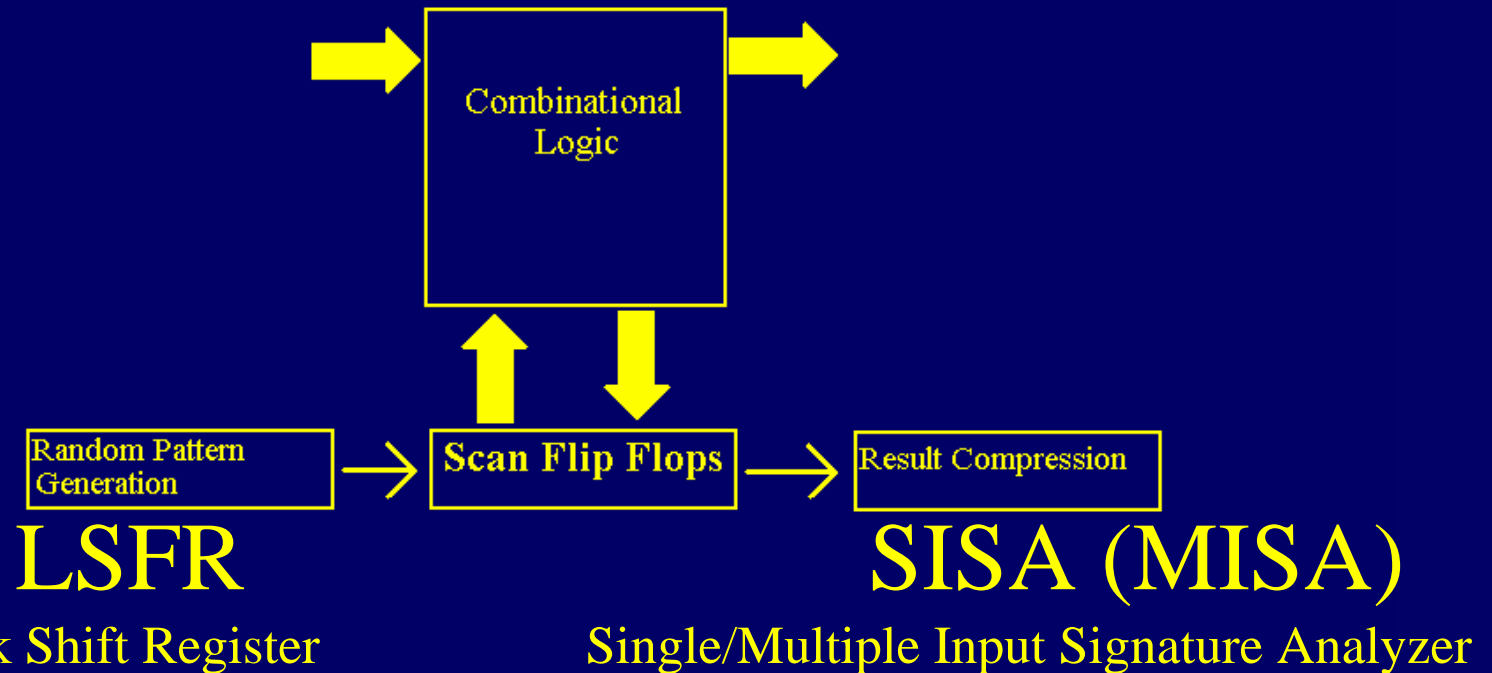
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# Scan Based Logic BIST

- Industry Standard

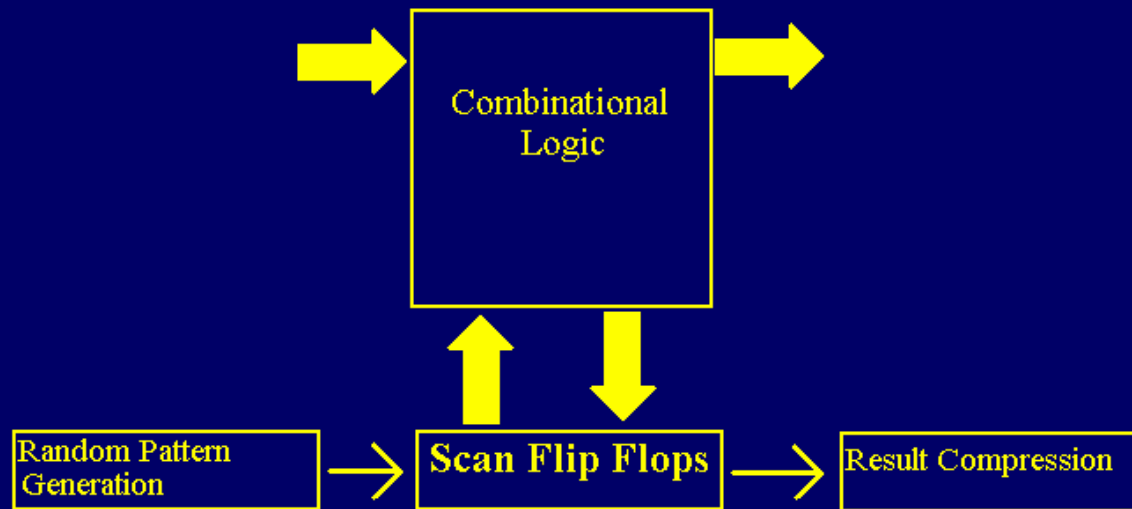


# Scan Based Logic BIST

>>> Attractive solution for Core test

- Minimal need for test access busses
  - Can be supported by IEEE 1149.1
- Can run complete BIST test as specified by the core provider (for “hard” cores)
  - Fault Simulations models are not needed by SoC integrator >> Protects IP

# Scan Based Logic BIST

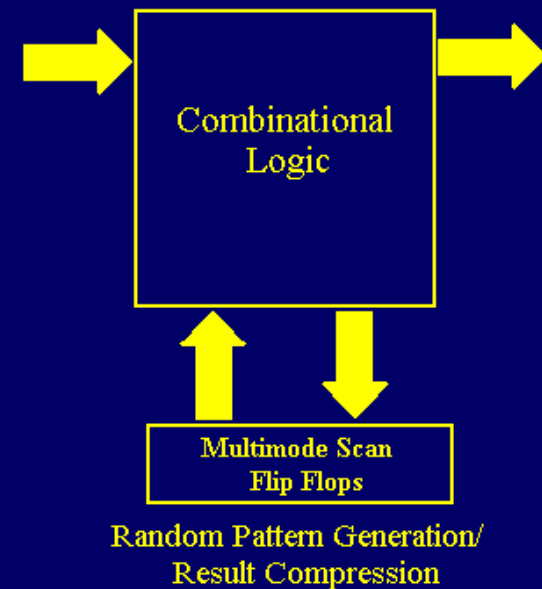


Two **serious** limitations:

- Slow test-per-scan test execution
- Very limited support for two/multiple vector delay tests

# Multi-Mode Scan: *Test-per-Clock* BIST

- Employs Circular BIST
- Combines test generation/results compression in FFs
- Retains ALL benefits of scan based logic BIST
- Fast test-per-clock operation
  - > 2 orders of magnitude faster
- Many other advantages

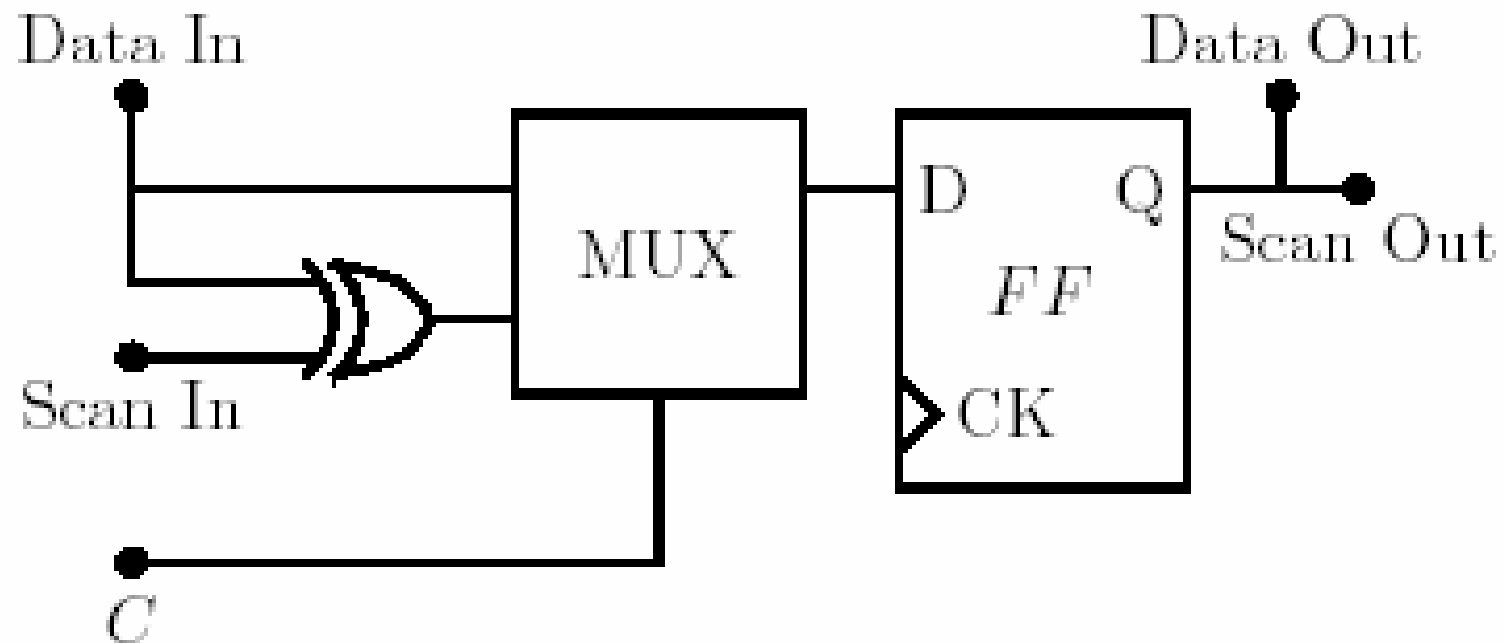


# Circular BIST

## The Basic Idea:

- Suppose we scan in a random state into the circuit flip-flops as an initial state
- Now if we EXOR the next circuit state with this shifted random initial state, we will essentially get another random state vector

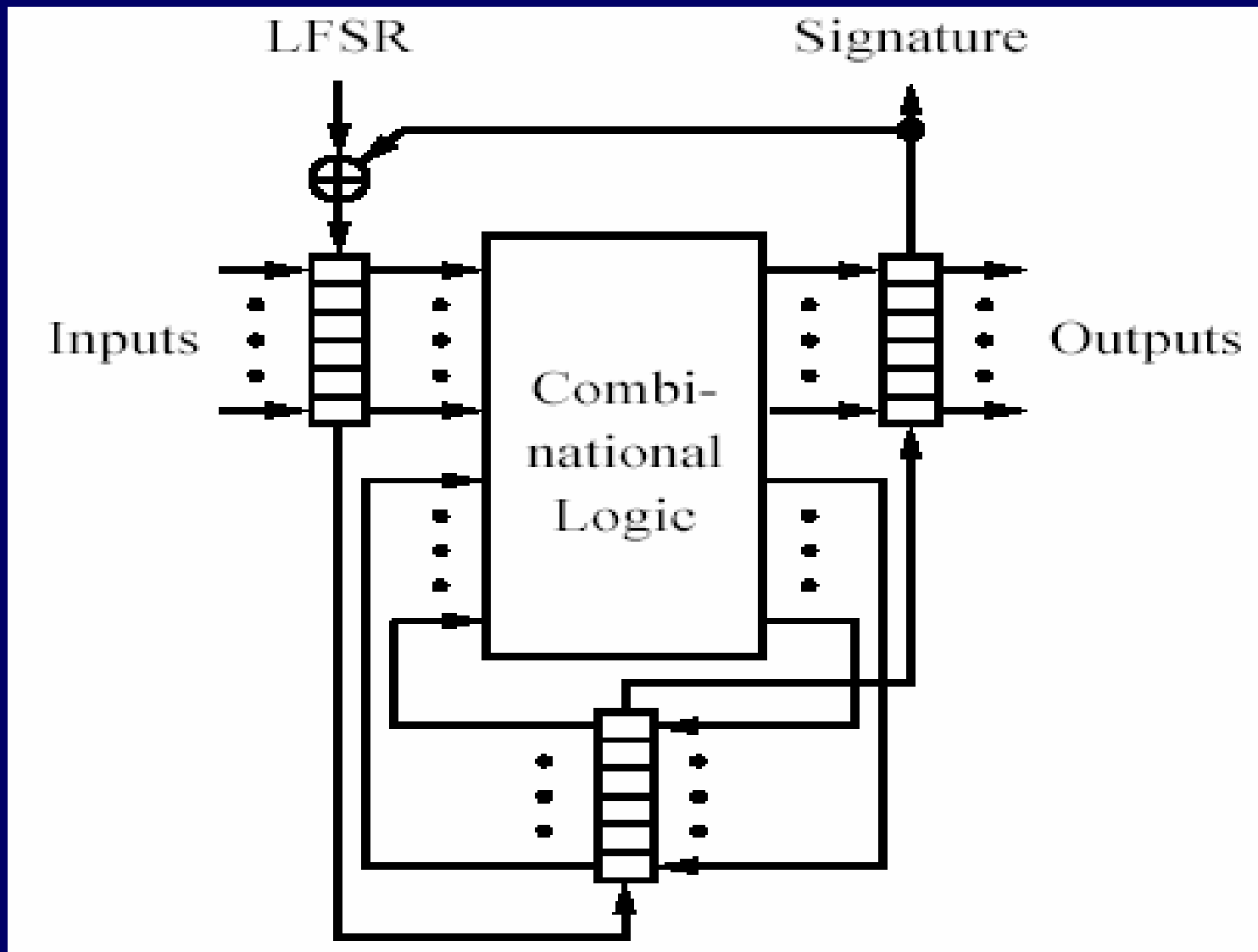
# Circular Self Test Path (CSTP)



Modes	$C$
System	0
Test	1

Fig. 6. Circular Self Test Path Memory Element[10]

# Pseudorandom Circular Self-Test



# Circular Self Test Path (CSTP)

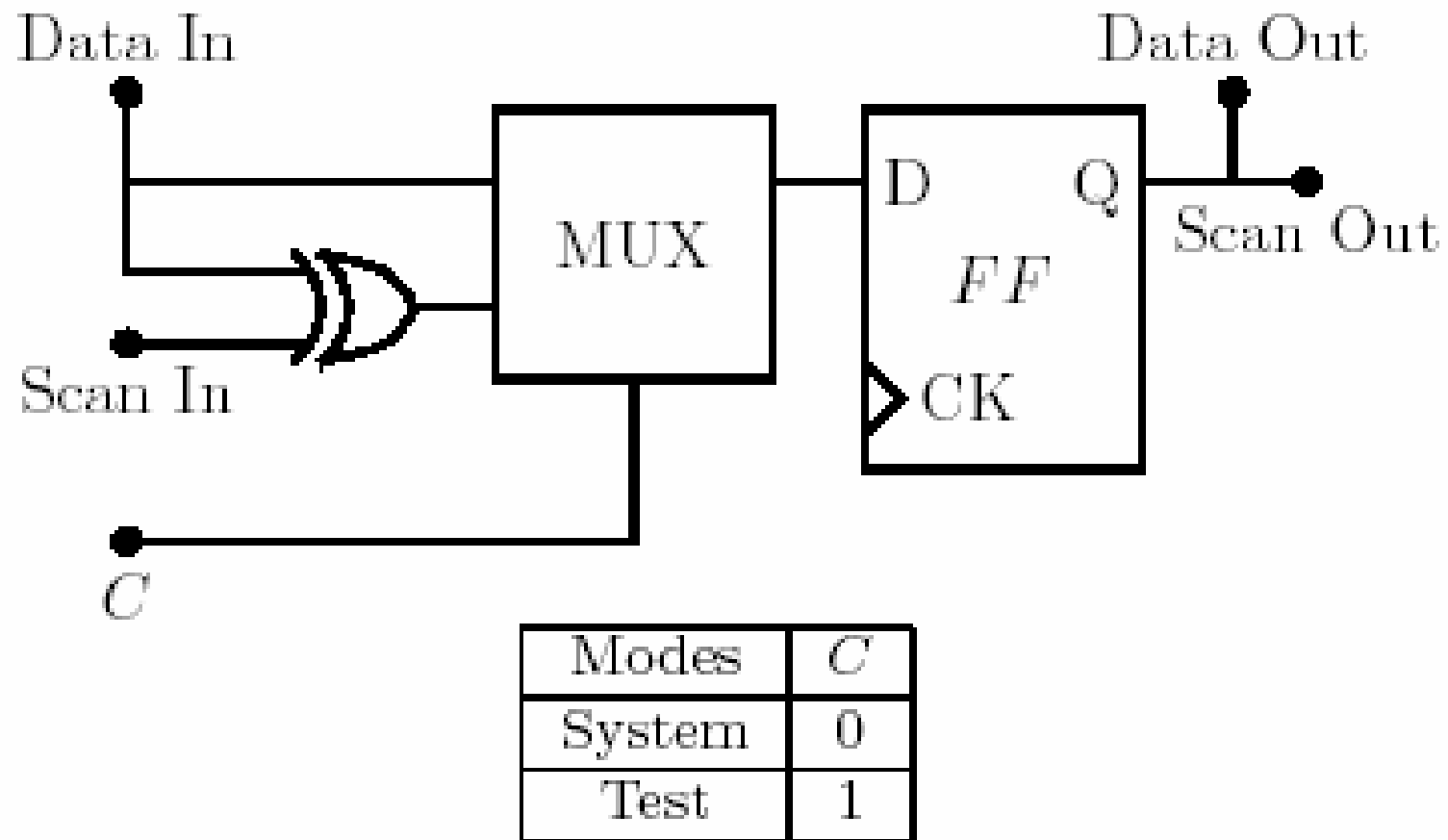
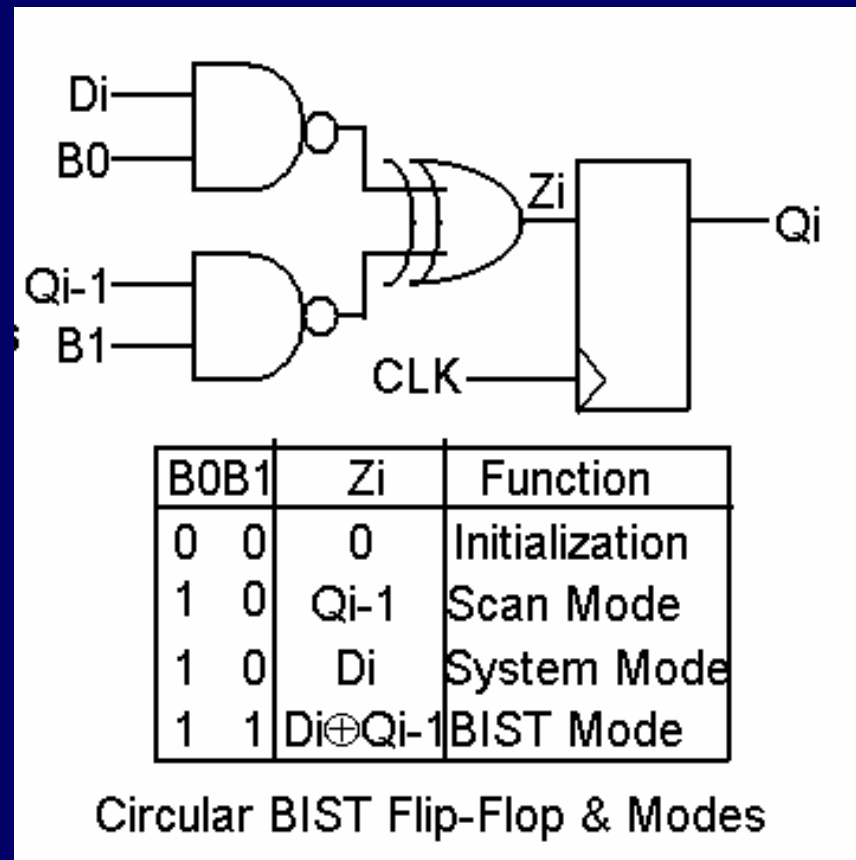


Fig. 6. Circular Self Test Path Memory Element[10]

# Overview of Circular BIST

- Replace existing flip-flops with CBIST flip-flops
- Connect CBIST flip-flops to form circular chain
- Isolate system data inputs for reproducible results
- Add test controller to control BIST sequence
  - Initialization
  - BIST mode
  - Read signature
  - Return to system mode



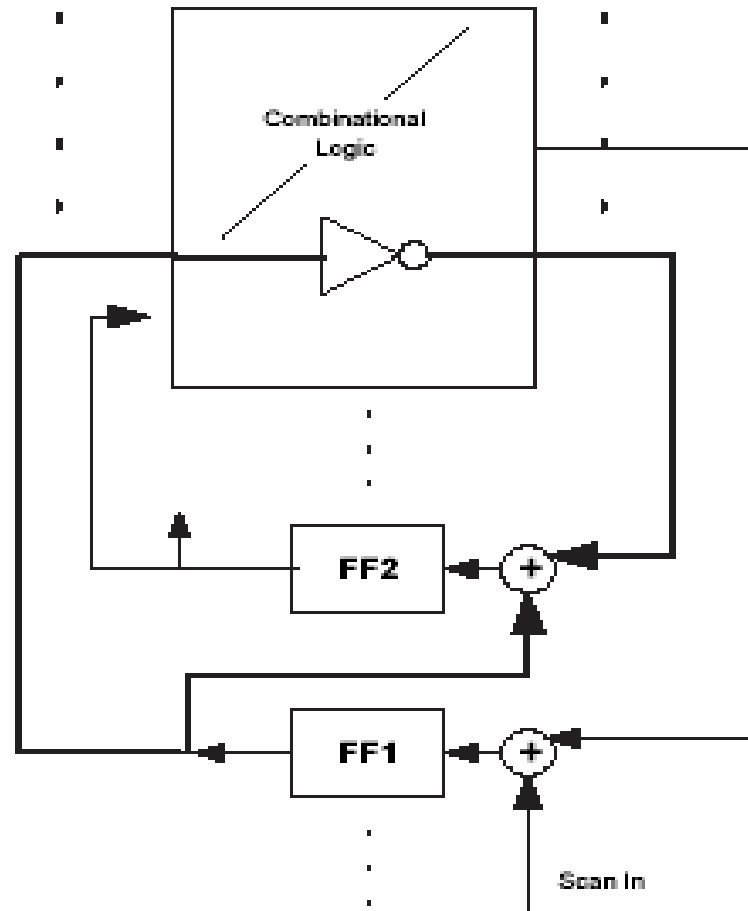
# Overview of Circular BIST

- Easy to create CAD tools for BIST synthesis
- *Vertical testability* (from wafer to system level)
- High fault coverage (typically  $> 90\%$ )
- Scan mode for augmenting fault coverage
- At-speed testing
- Low area & performance penalties
  - typically 10% to 20% additional logic
  - 2 to 3 gate delays
  - Control by selective replacement
- Also known as Circular Self-Test Path (CSTP)

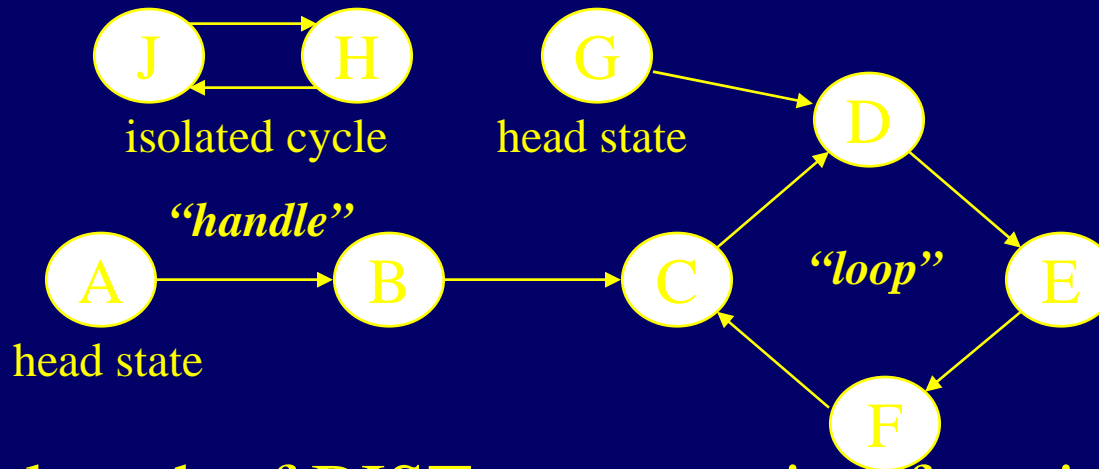
# Problems with Circular BIST

- Low fault coverage in some circuits due to:
  - Register adjacency
    - Worst when  $D_i=Q_{i-1}$  then  $Z_i$  is always logic 0
    - Can occur whenever  $D_i=f(Q_{i-1})$
    - Compacted data containing fault information is lost unless the bit(s) can propagate through the circuitry under test
    - avoid by ordering CBIST chain
  - Limit cycling
    - due to the closed nature of CUT in BIST mode
    - also function of initialization state

# Register Adjacency



# Limit Cycling in Circular BIST

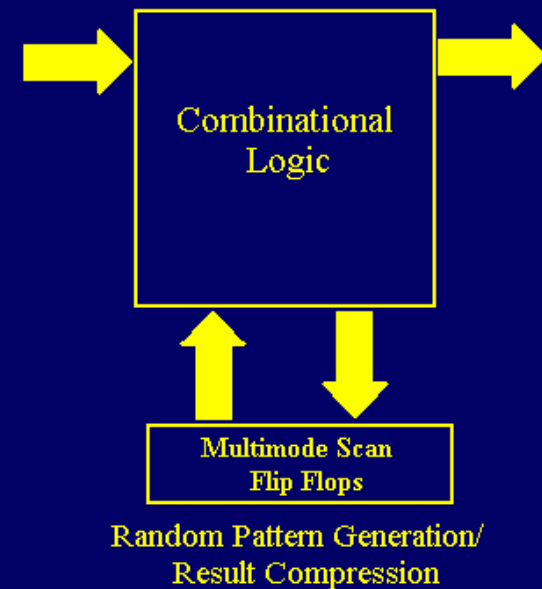


- Cycle length of BIST sequence is a function of:
  - Initialization value
  - State Transition Graph
- Once a loop is entered, the sequence repeats
- Head states can maximize cycle length (Prinetto et.al., ITC'94)
- Circuit under test may never visit all states
- few state transitions => few test patterns => low fault coverage

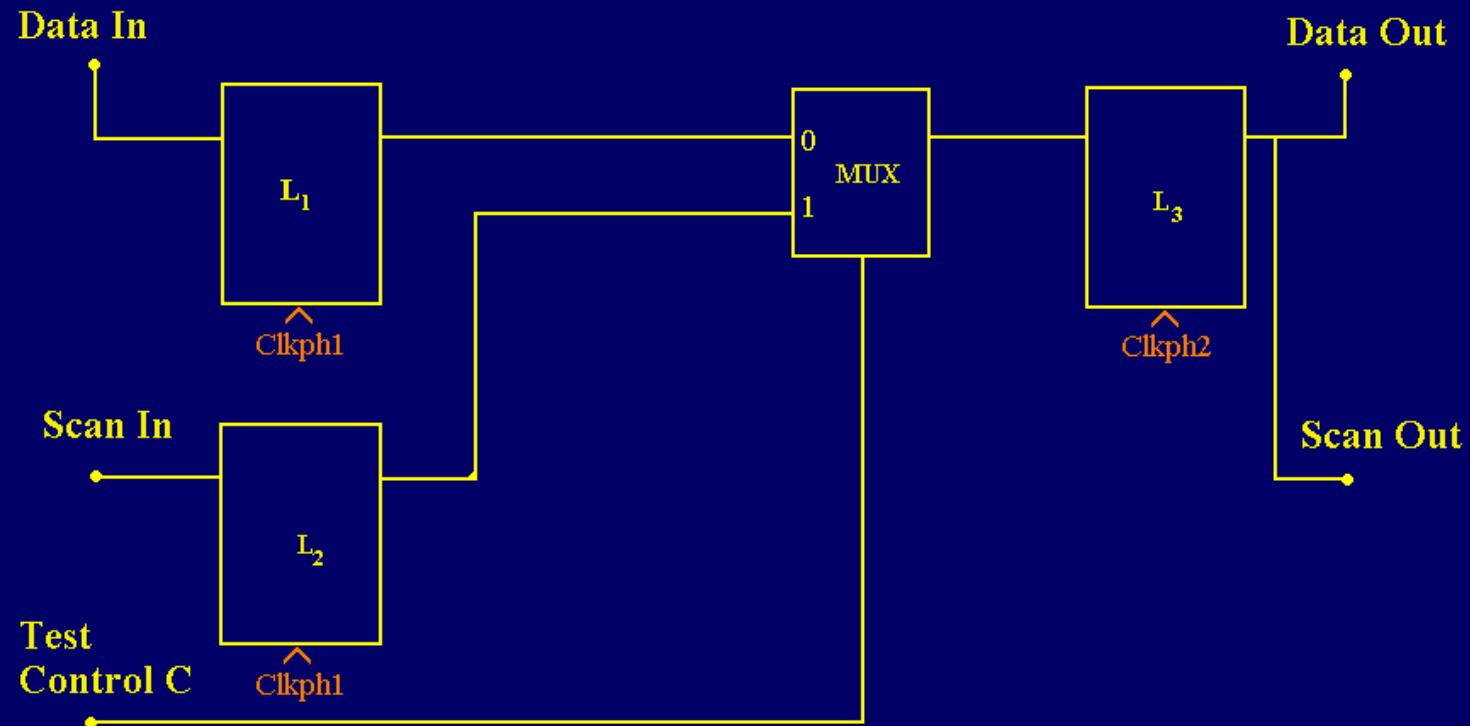
# Multi-Mode Scan: *Test-per-Clock* BIST

- Combines test generation/results compression in FFs

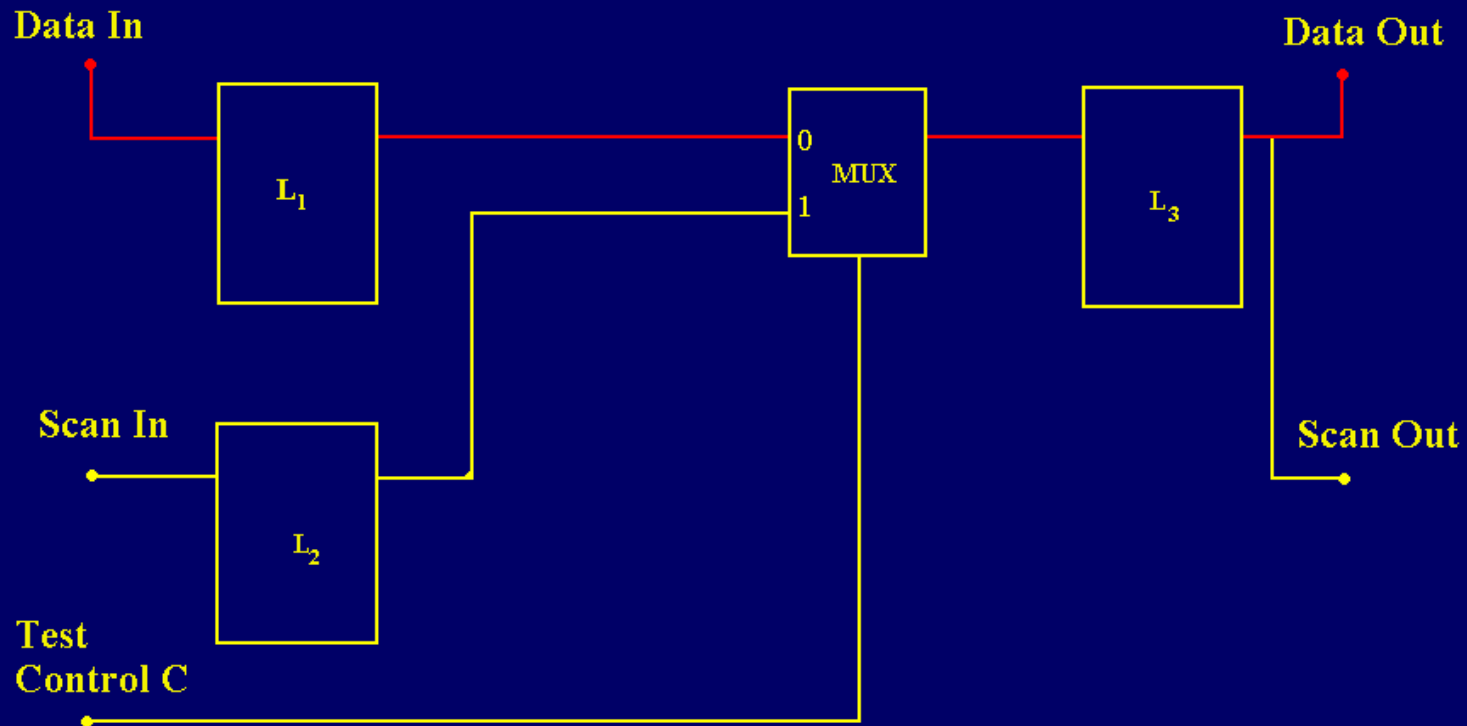
- Retains ALL benefits of scan based logic BIST
- Fast test-per-clock operation  
> 2 orders of magnitude faster
- Improved fault coverage
- Rich two and multi-pattern delay tests



# Conceptual Schematic for Classical Scan

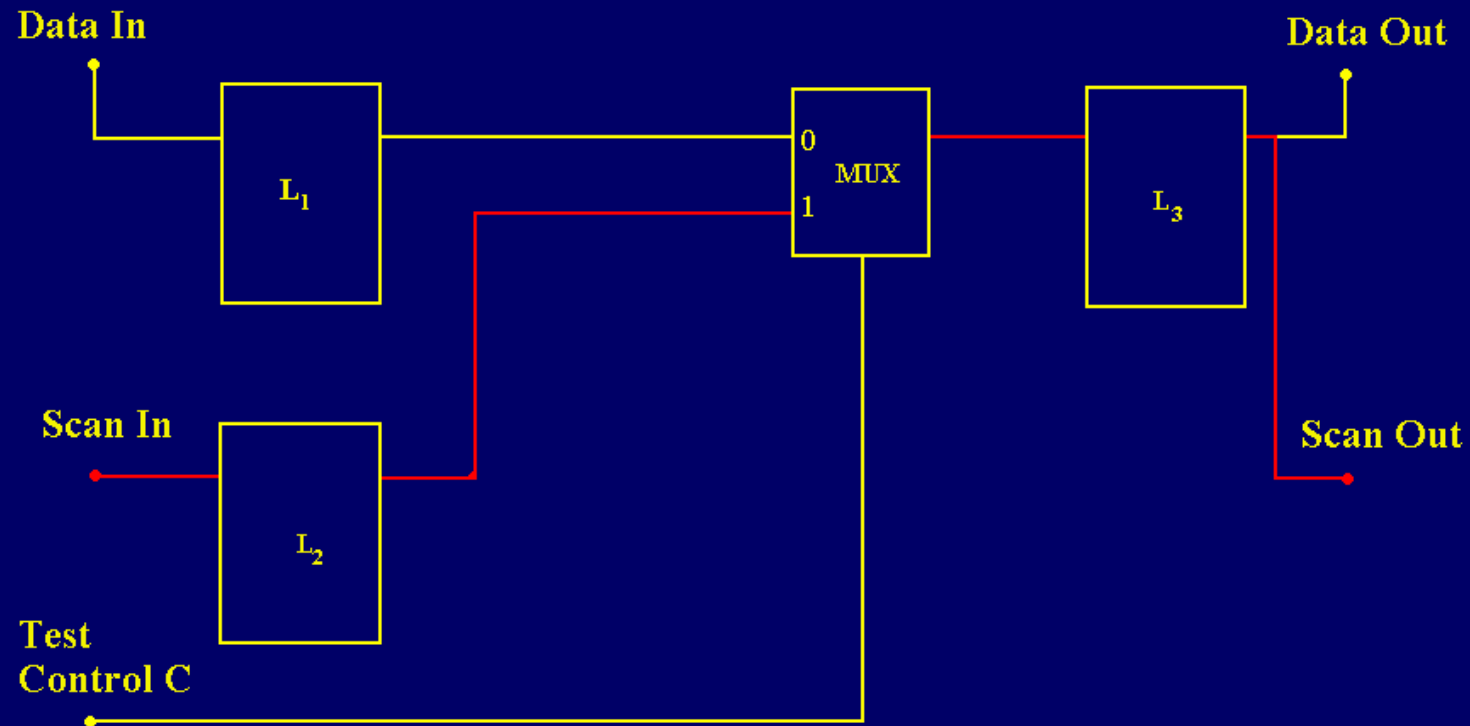


# Conceptual Schematic for Classical Scan



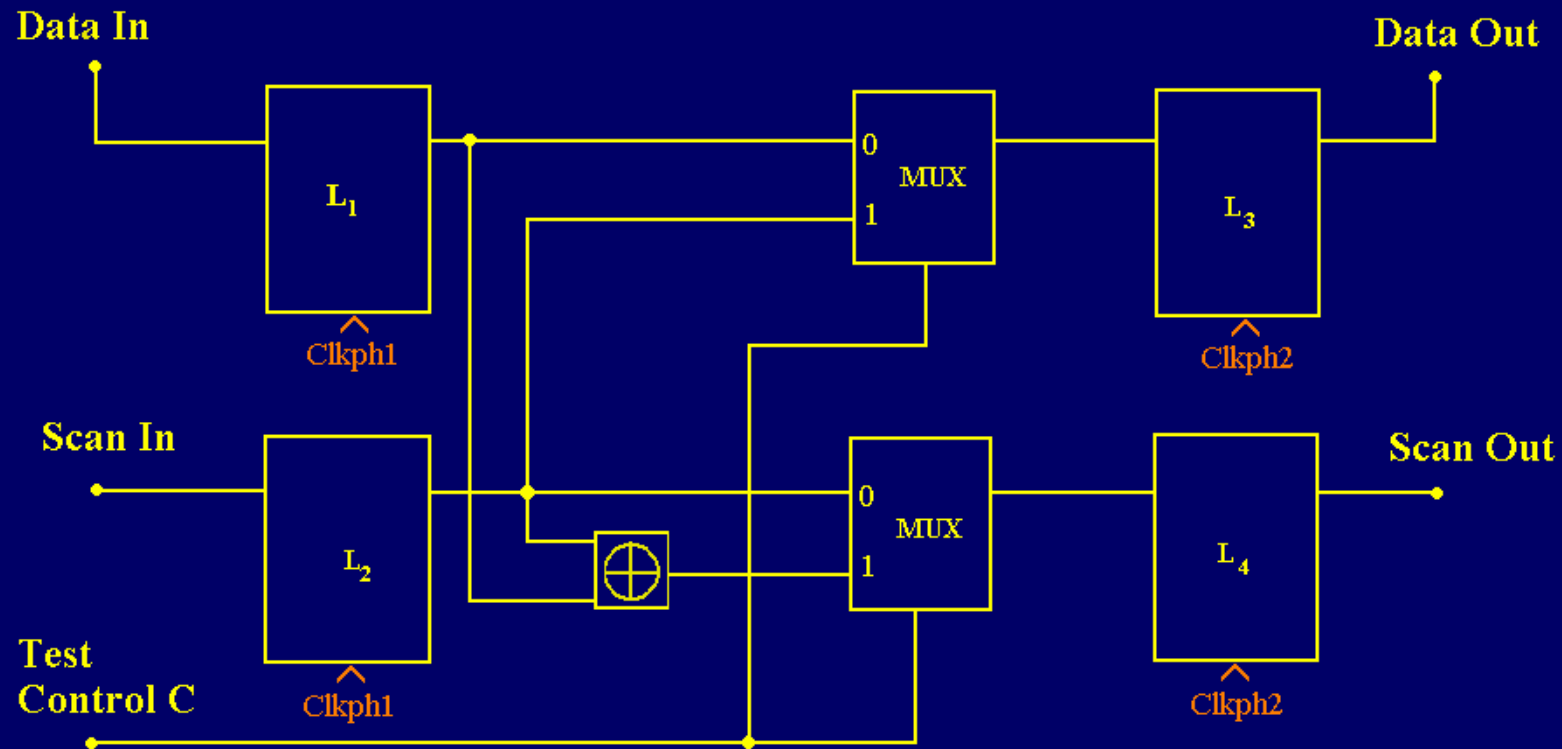
Normal functional operation ( $C=0$ )

# Conceptual Schematic for Classical Scan

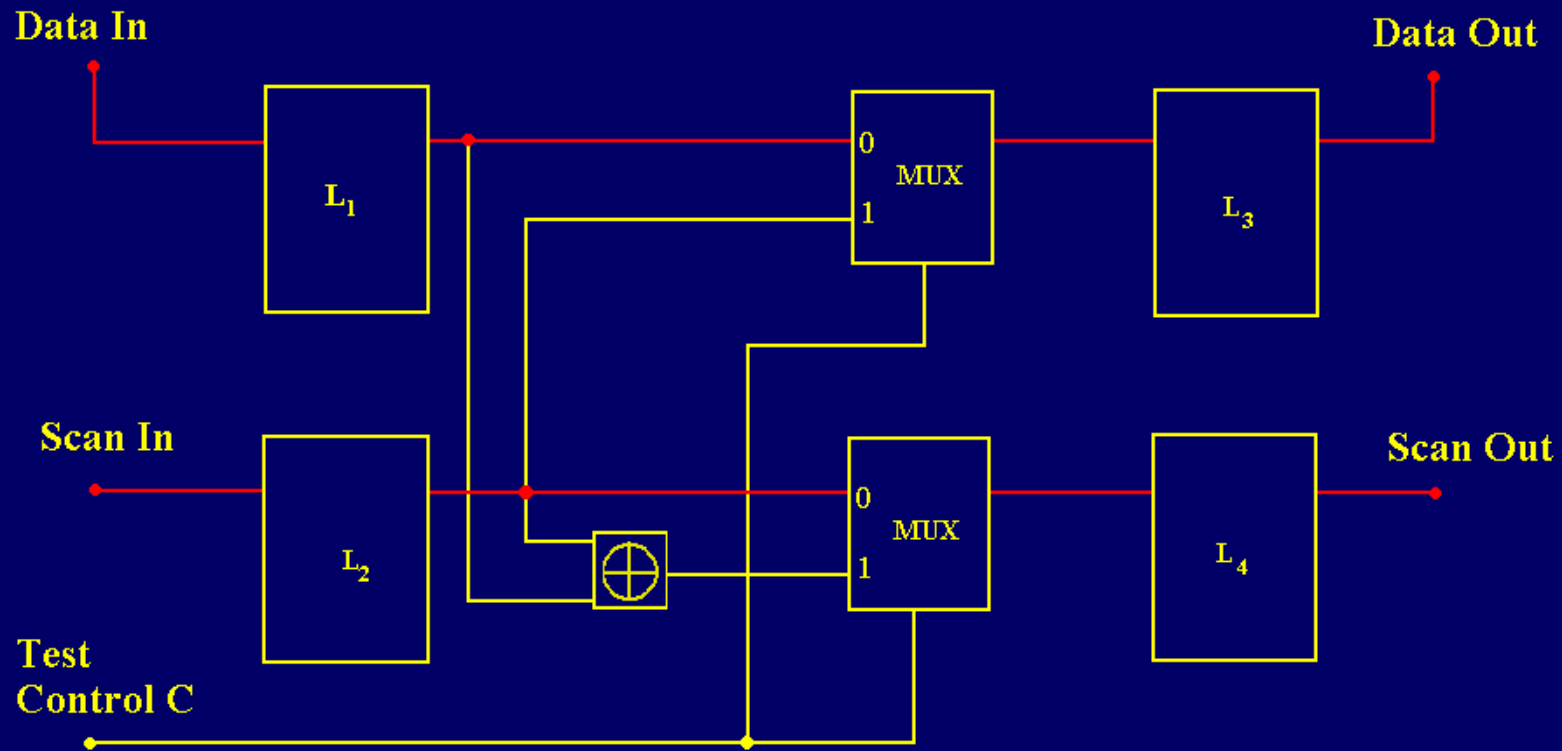


Scan shift operation ( $C=1$ )

# Multi-Mode Scan Memory Element

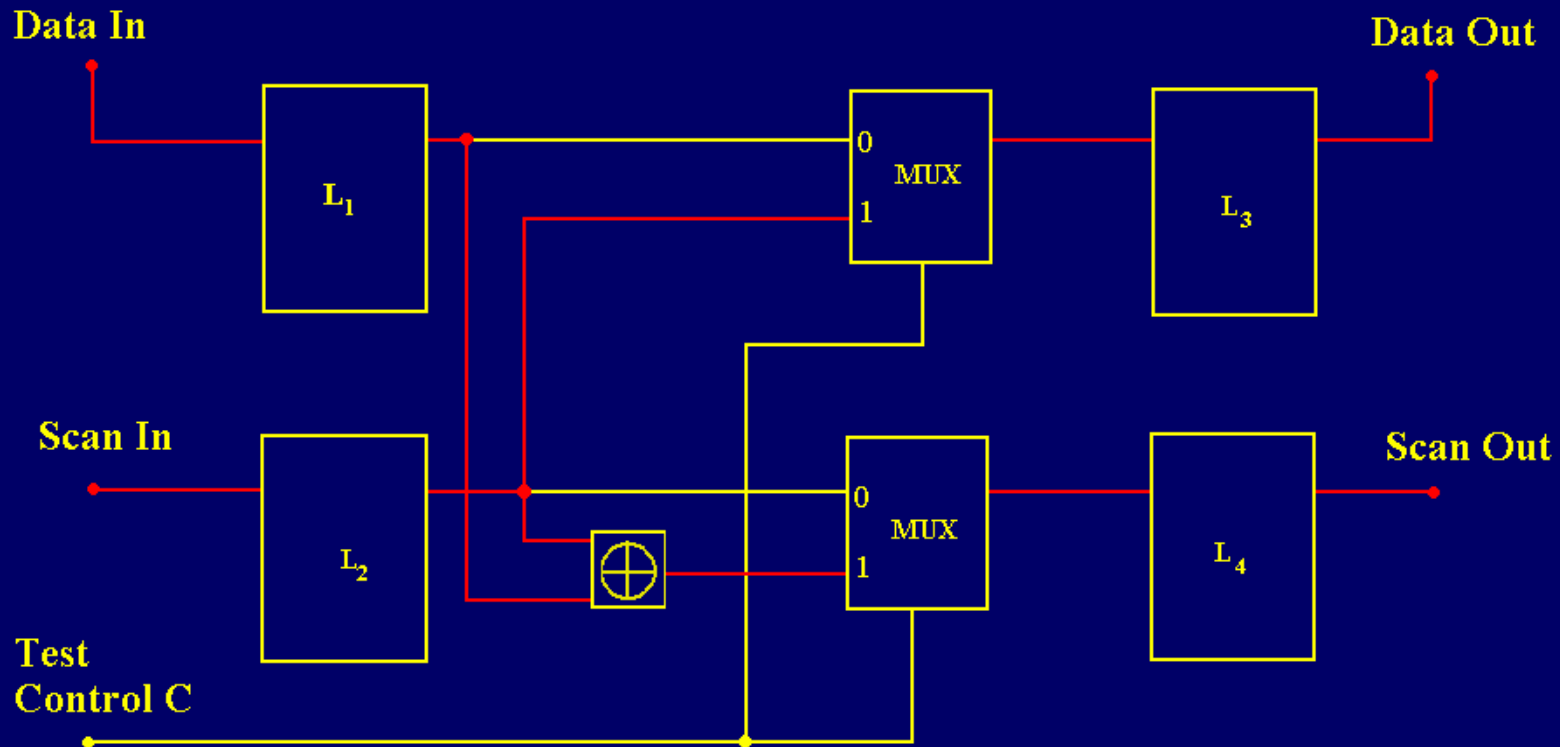


# Multi-Mode Scan Memory Element



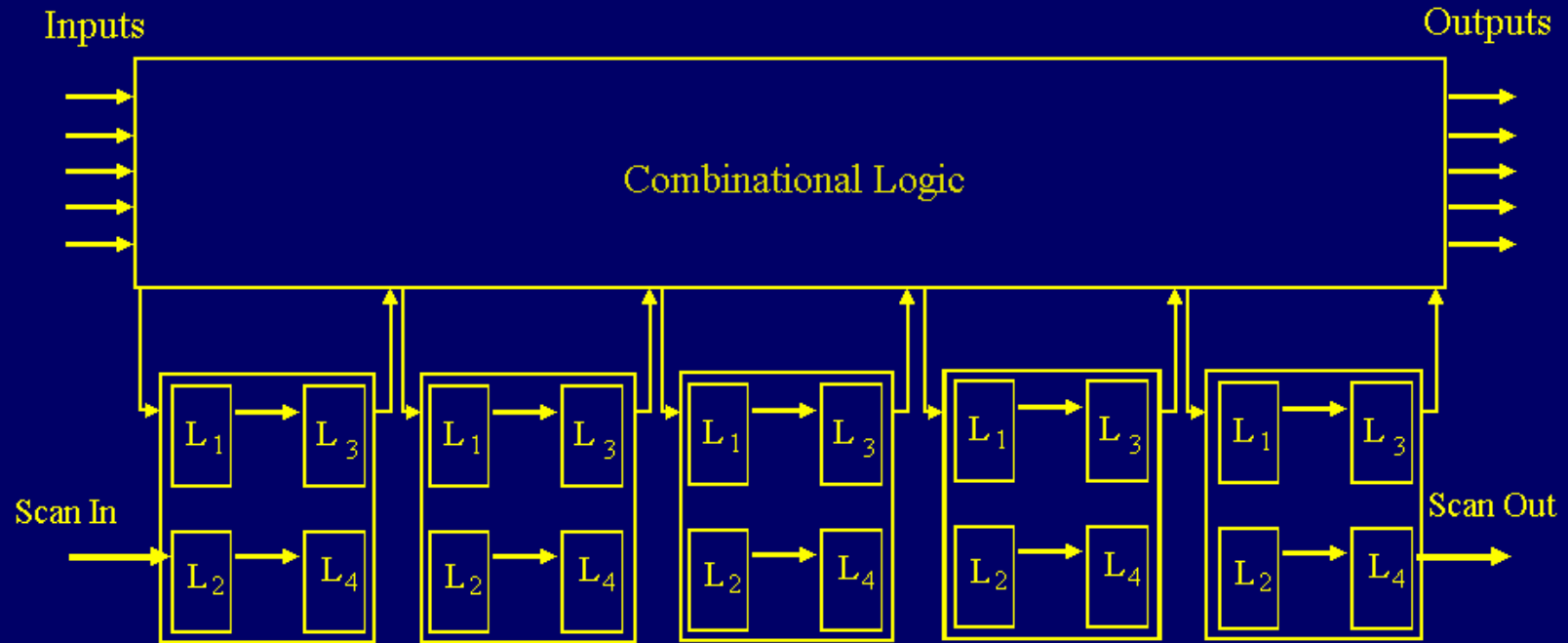
Normal Operation/Scan Shift (C=0)

# Multi-Mode Scan Memory Element

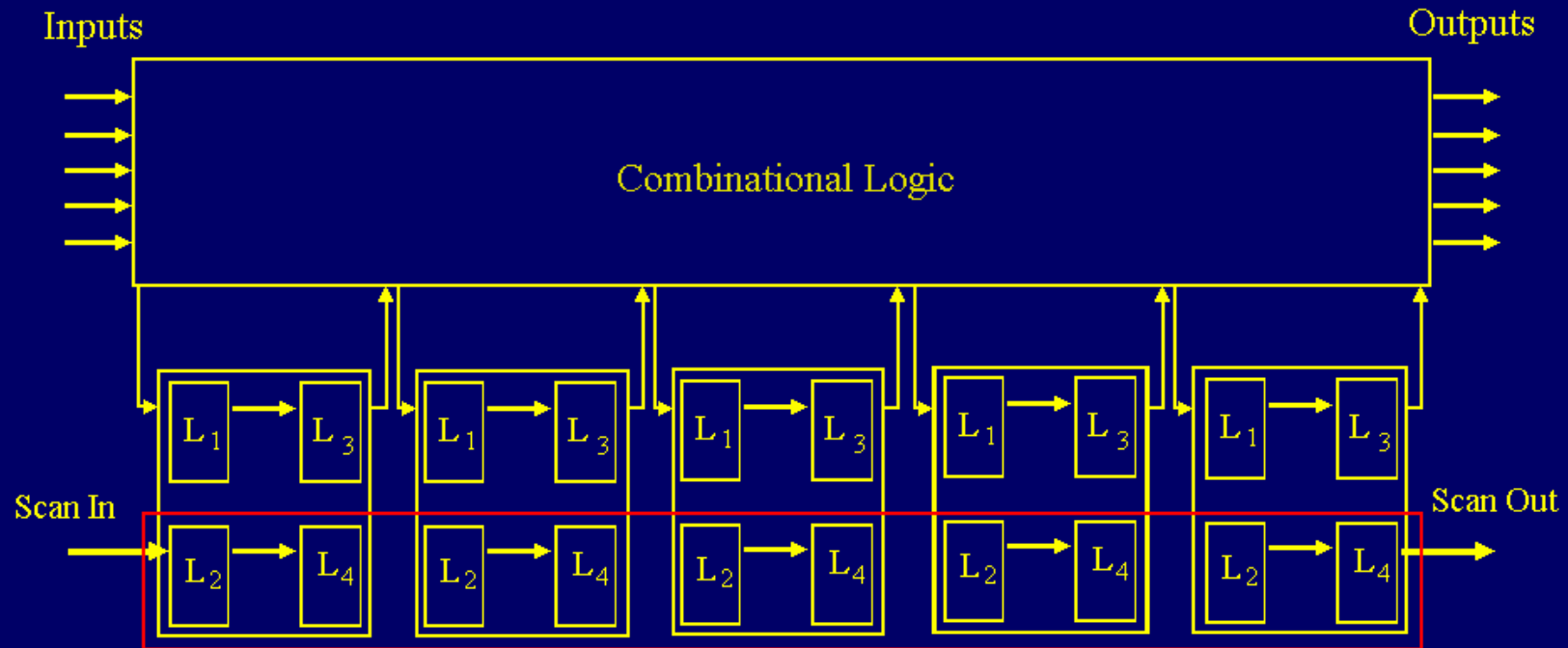


Pseudorandom Self-Test (C=1)

# Normal Operation/Scan Shift Mode



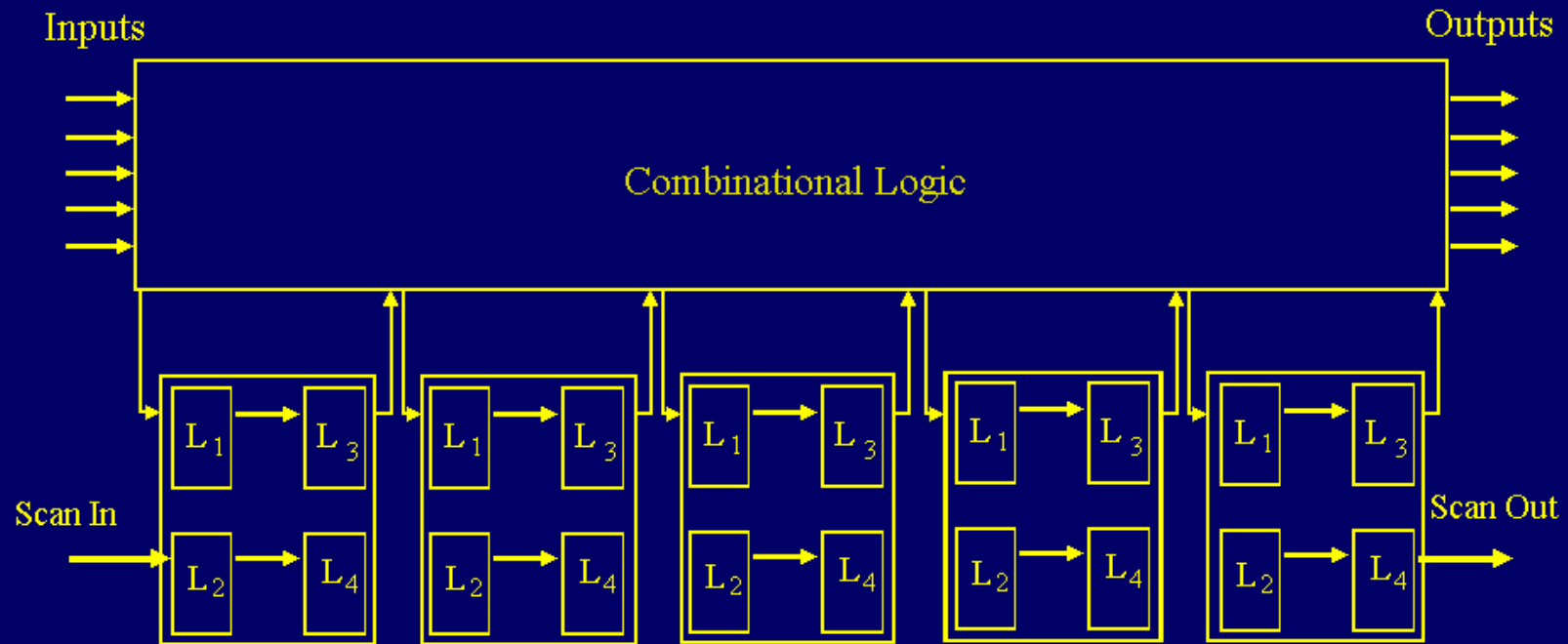
# Normal Operation/Scan Shift Mode



Independent Scan Register

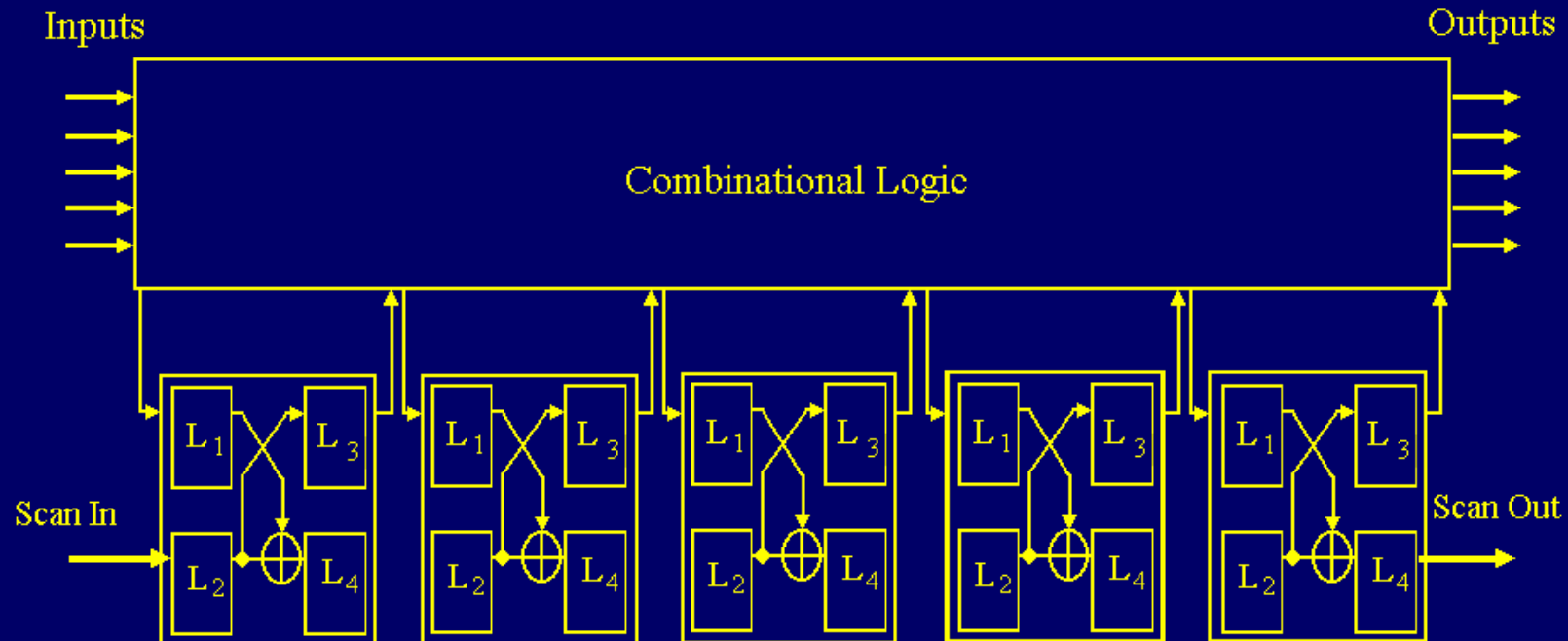
- SCAN/MISA Register

# Normal Operation/Scan Shift Mode



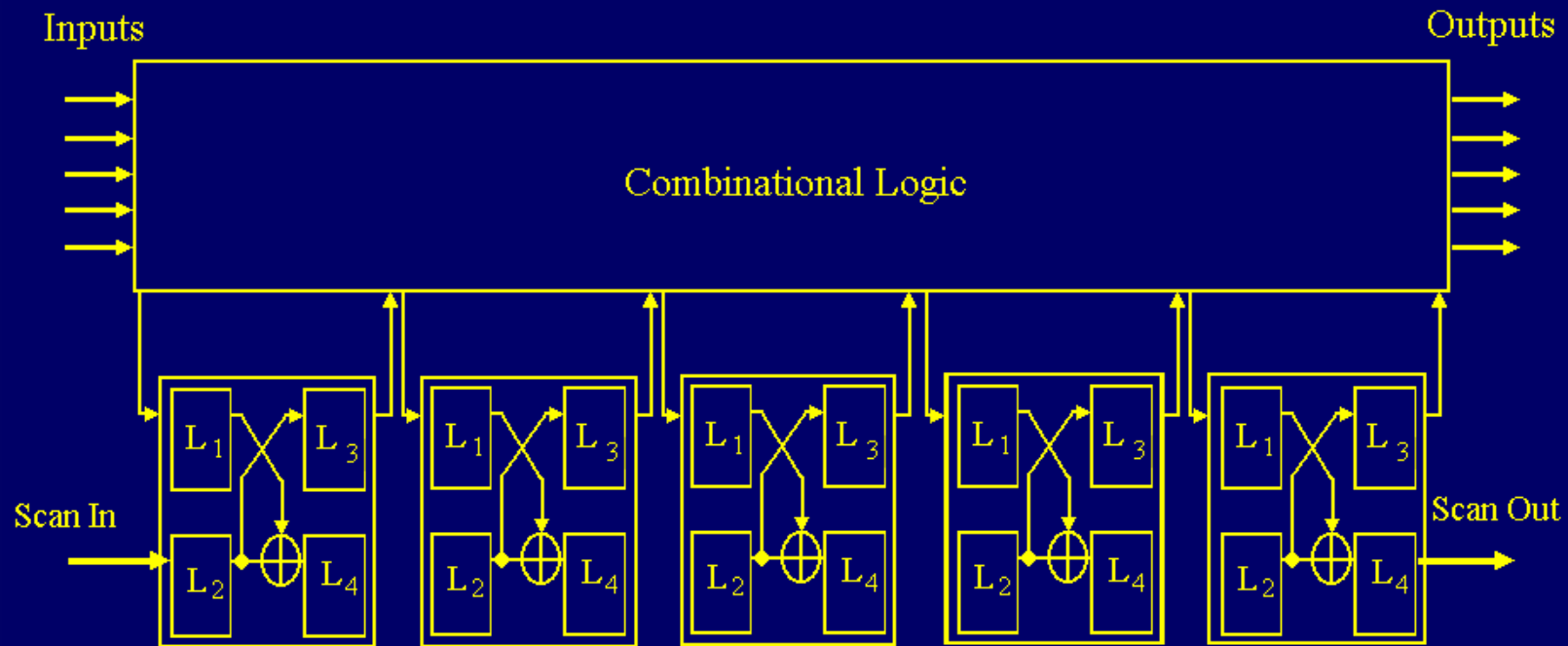
Note: No switching activity in the scan chain if Scan-In is held steady at 0 (or 1)

# Pseudorandom Self-Test Mode



- Scan/MISA Register provides state input
- Next state vector is accumulated (modulo 2) in (shifted) Scan/MISA Register
- Rich random patterns in Scan/MISA Register

# Pseudorandom Self-Test Mode



- Test-per-clock operation in self-test mode
- Random patterns in Scan/MISA Register provide rich 2-pattern and multi pattern tests
- Actual functional paths tested for timing delays

# Register Adjacency

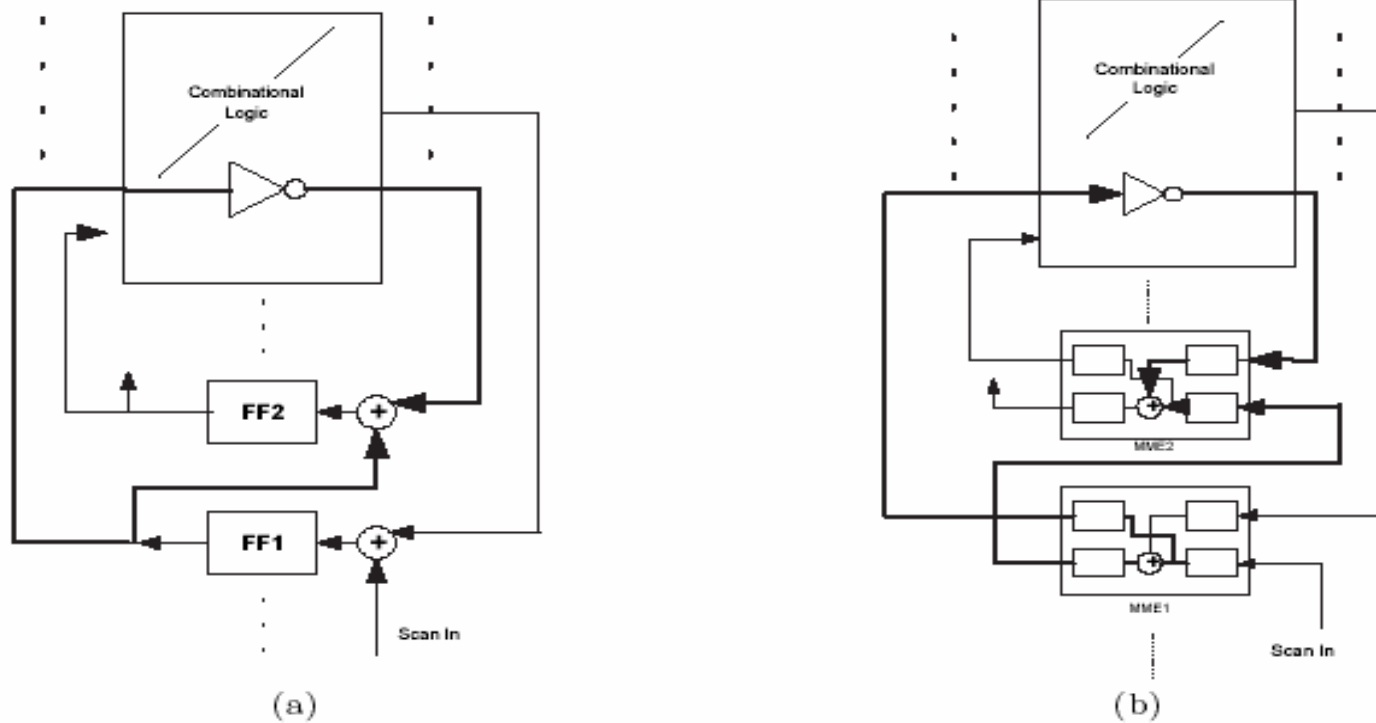
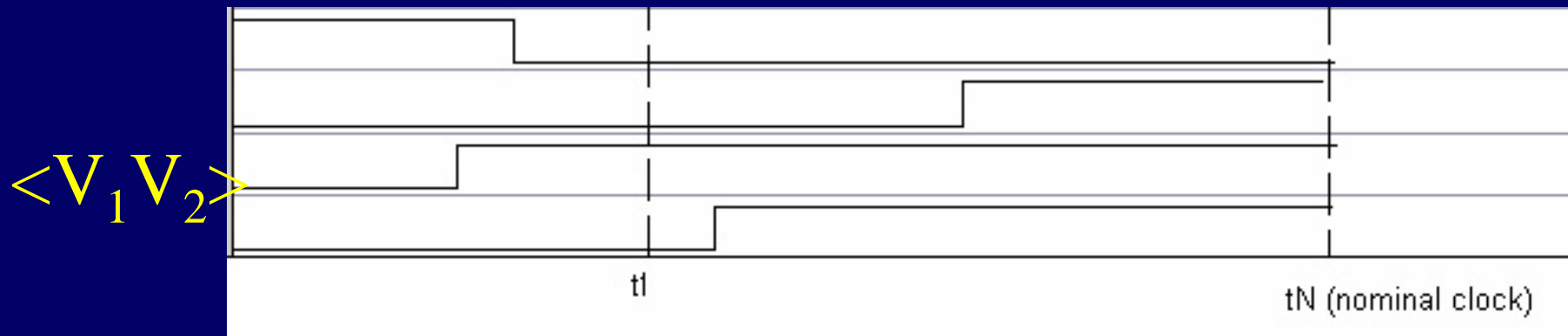


Fig. 7. State Dependencies in (a)CSTP and (b)MME Designs

# Timing Tests



$V_1$        $V_2$

- Two sequential test vector inputs  $\langle V_1 V_2 \rangle$  cause a change at an output
- The switching delay is the time from the application (launch) of  $V_2$  until change at the output

# Scan Based Delay Testing

# Launch-on-Shift

## LOGIC

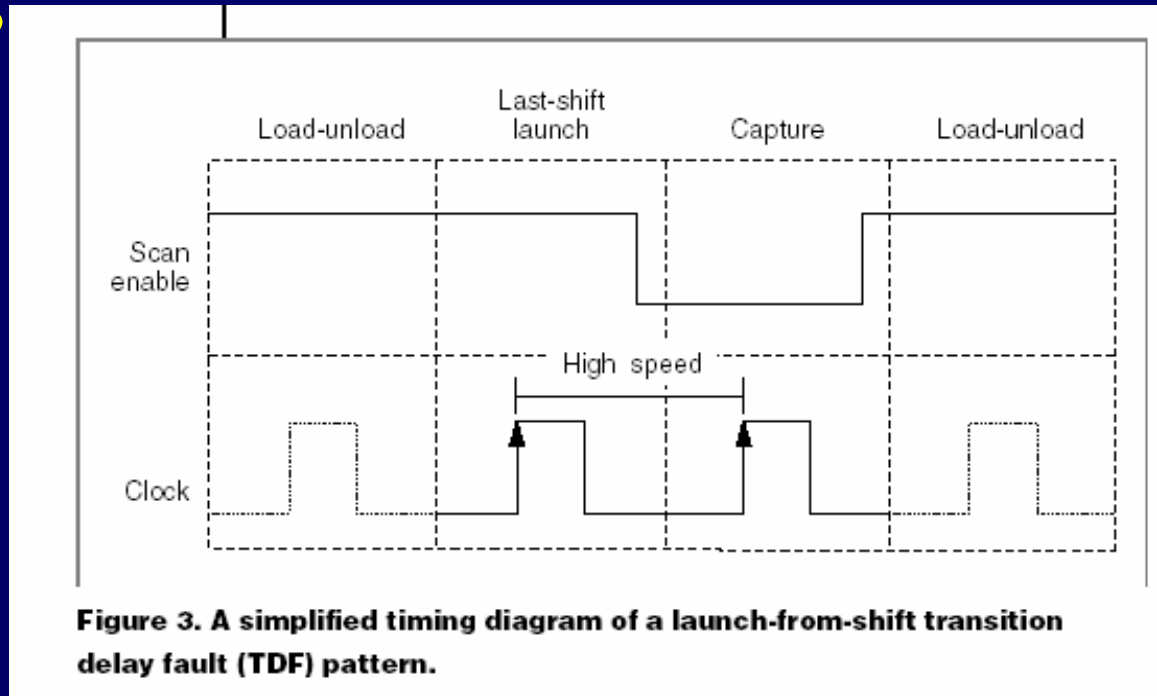
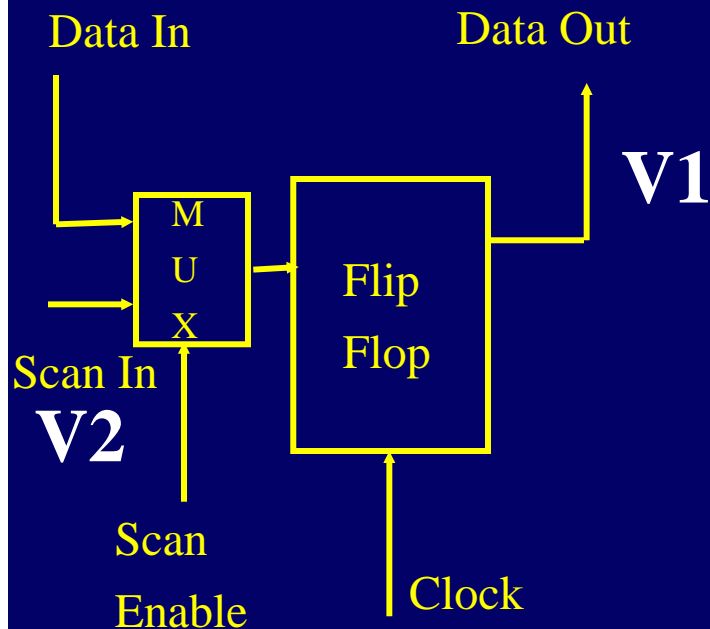


Figure 3. A simplified timing diagram of a launch-from-shift transition delay fault (TDF) pattern.

Clock Edge 1: Launch V2 (scan = 1)

Then switch scan = 0

Clock Edge 2: Capture response to V1 > V2 change in Flip Flop

# Scan Based Delay Testing

# Launch-on-Capture

## LOGIC

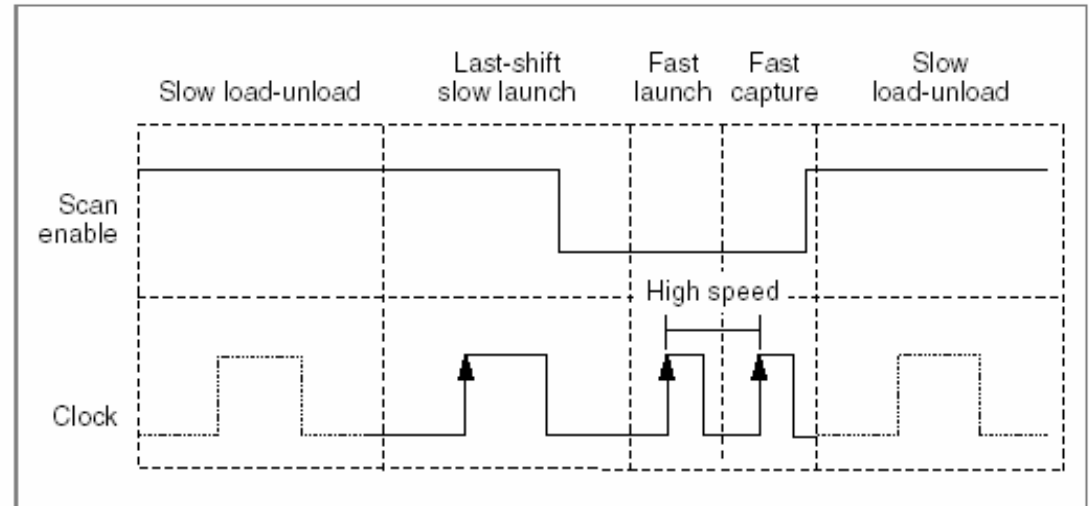
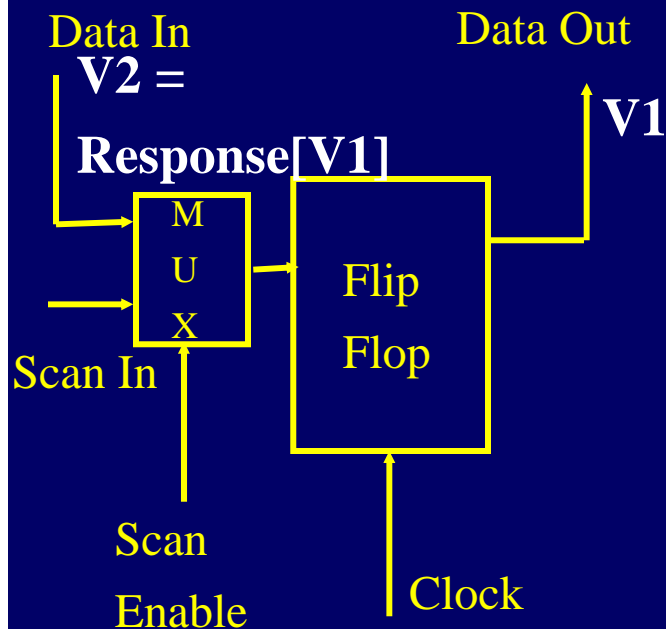


Figure 4. Simplified timing diagram of a launch-from-capture (broadside) TDF pattern.

Clock Edge 1: Apply  $V1$  (scan = 1)  
Then switch scan = 0

Clock Edge 2: Capture response to  $V1$  in  
Flip Flop to launch timed  
transition. This is  $V2$

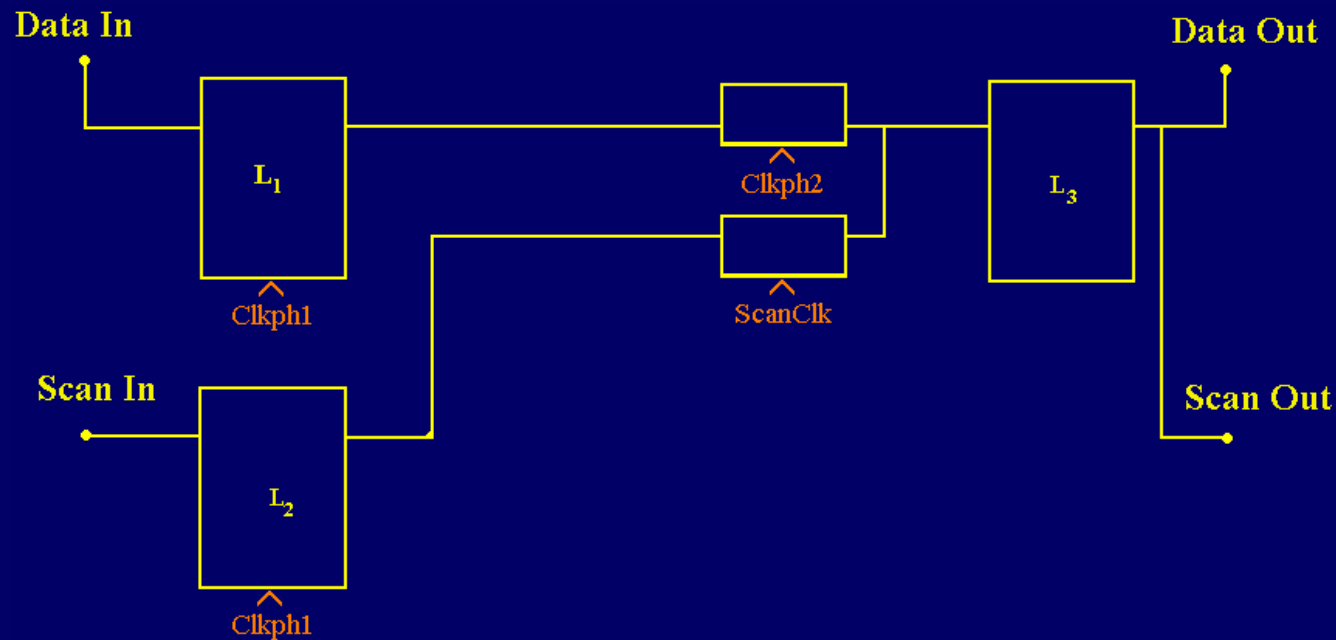
Clock Edge 3: Capture response to  $V2$

# Simulation Results for Transition Delay Fault Coverage

Curcuit under test	Indep vectors	100,000 B-side test	patterns Scan (S-load)	MME Self-Test	Scan S+B	200,000 Scan S+B+ Reorder	patterns MME Self-Test	MME Mode-Switch
s208	100	76.59	90.46	100	94.51	94.8	100	100
s298	100	79.33	82.28	100	94.09	99.02	100	100
s344	100	94.57	94.38	100	98.18	100	100	100
s349	99.12	93.64	93.64	99.09	97.17	99.11	99.09	99.09
s382	100	77.4	91.02	100	93.81	98.61	100	100
s386	100	76.81	83.91	90	94.2	95.65	90.15	100
s400	98.26	76.16	89.68	98.26	92.44	96.51	98.26	98.26
s420	96.53	71.97	83.82	89.61	92.78	94.51	95.53	97.63
s444	96.99	74.35	84.69	96.73	91.23	95.94	96.73	96.99
s510	100	89.23	90.48	100	96.65	97.39	100	100
s526	99.9	62.24	86.39	99.9	92.62	96.62	99.9	99.9
s641	97.96	96.73	98.09	97.12	98.23	98.37	97.12	99.04
s713	87.91	82.46	87.69	88.13	87.91	87.91	88.24	89.54
s820	100	80.5	84.94	98.86	92.82	92.82	99.11	100
s832	98.95	78.93	83.64	97.89	91.45	91.45	97.96	98.95
s1196	99.6	98.96	99.67	99.24	99.77	99.77	99.91	99.91
s1238	95.98	94.73	95.6	96.16	95.82	95.82	96.24	96.24
s1423	99.01	88.65	96.02	99.01	98.58	98.58	99.05	99.05
s1488	100	91.3	79.82	100	97.26	97.26	100	100
s1494	99.43	90.68	79.18	99.43	96.66	96.66	99.43	99.43
s9234	86.33	72.55	79.94	85.99	84.07	87.87	88.18	88.18
s13207	95.11	82.86	90.99	93.68	94.52	95.82	94.59	94.99
s15850	91.04	65.14	86.42	91.1	88.47	91.21	92.14	92.87
Average	97.48	82.43	87.6	96.53	94.05	95.73	97.03	97.83



# Implementation Issues



- Clock controlled standard scan less effective for delay testing
- Scan clock must be guard-banded for skews relative to clock phase 2

# Conclusions

- Multi-Mode Scan provides test-per-clock self-test
- Rich mix or random vectors to support delay testing of true functional paths
- Minimal need for test access to core: IEEE 1149.1
- Supports traditional scan for diagnosis
- Ease of design: identical cell pin-outs as traditional scan

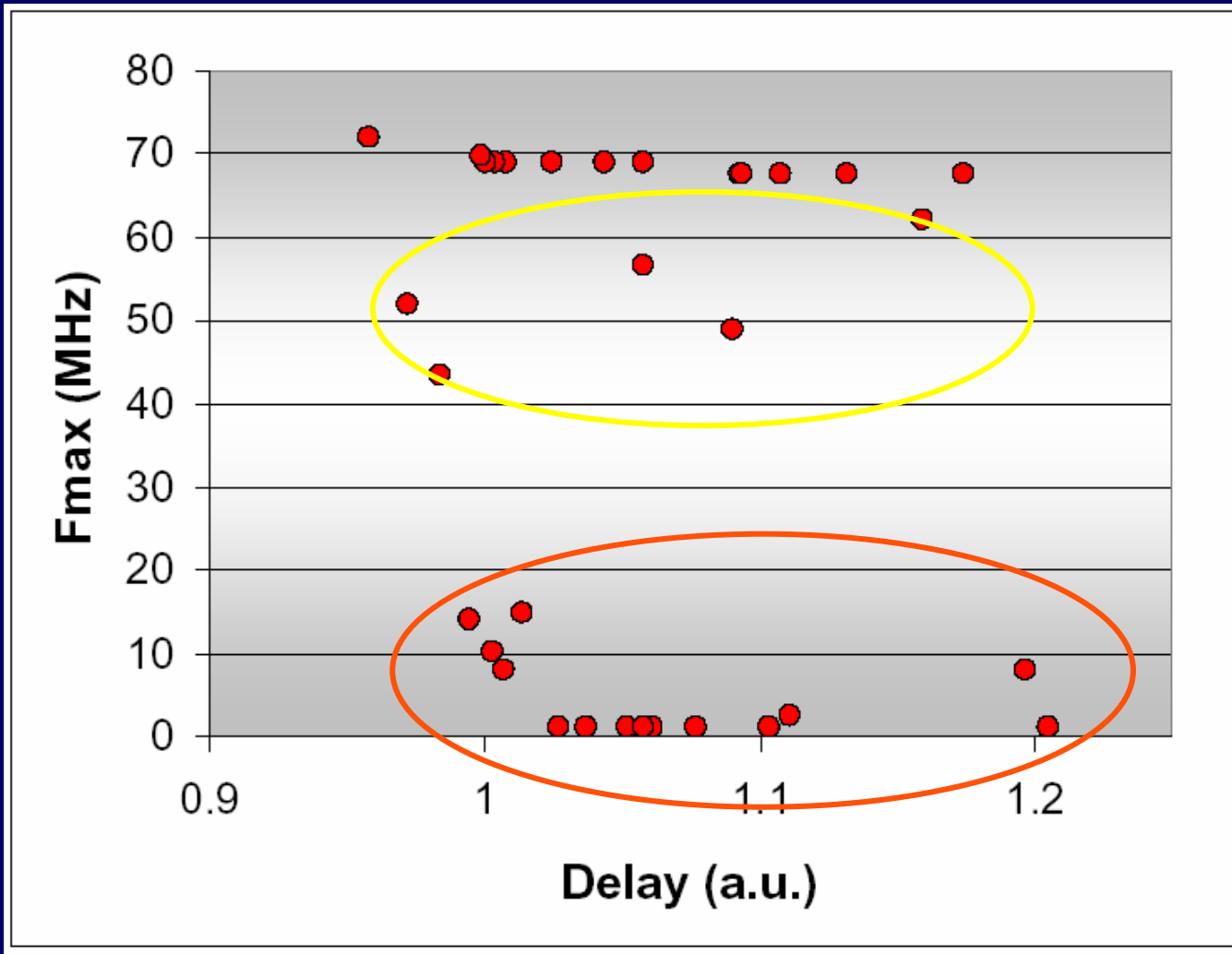
# Open Problems

- Handling large number of X-states
- Covering random pattern resistive faults
- Delay Testing
  - MMSCAN can efficiently support FMAX testing

# Fmax Testing

- Fmax Testing finds the highest clock rate for which a circuit passes a given (TDF) test set
- A binary search using repeated applications of the test set is performed to obtain Fmax
- An abnormal Fmax value compared to other circuits from the lot indicates a defect that may cause a functional or reliability failure in the field

# Fmax Testing



Intrinsic  
← Clock

Operation  
← al Clock

Fmax for TDF pattern for 32 parts that pass dc tests but fail system level tests [1]

# Fmax Testing

- Fmax outliers may experience a delay failure in the field because delay test sets often cannot test worst case signal propagation conditions
- Fmax outliers may also contain latent defects that can cause early life failure

Questions?