

Title : Hierarchical Fault Collapsing for Logic Circuits
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Abstract :

Firstly, we discuss fault equivalence and dominance relations for multiple output circuits. The conventional definition for equivalence says that “two faults are equivalent if and only if the corresponding faulty circuits have identical output functions.” This definition, which is based on indistinguishability of the faults, is extended for multiple output circuits as “two faults of a Boolean circuit are called equivalent if and only if the pair of the output functions is identical at each output of the circuit.” This is termed as diagnostic equivalence in this thesis. Alternatively, “if all tests that detect a fault also detect another fault, not necessarily at the same output, then the two faults are called detection equivalent.” Two detection equivalent faults need not be indistinguishable.

The definitions for fault dominance follow on similar lines. A novel algorithm based on redundancy identification is proposed to find the complete equivalence and dominance collapsed sets based on diagnostic and detection collapsing. Applying the algorithm to a 4-bit ALU collapses the total fault set of 502 faults to 253 and 155, respectively, according to diagnostic equivalence and dominance. The collapsed sets have 234 and 92 faults, respectively, for detection equivalence and dominance. In comparison, the traditional structural equivalence and dominance collapsing results in 301 and 248 faults, respectively.

Since functional fault collapsing using the proposed algorithm is time consuming, it is done for standard cells and other small logic blocks and saved as library information. This library is used for collapsing the faults of any circuit described hierarchically. We thus develop a hierarchical fault collapsing procedure. Using the redundancy-based fault collapsing for a full adder library cell, we hierarchically collapse faults in a 64-bit adder to sets of 1538 equivalence and 768 dominance collapsed faults. In comparison, a flattened 64-bit adder circuit collapses into 2306 structural equivalence and 1794 structural dominance collapsed faults. It is also shown that hierarchical collapsing can be done in CPU time which is an order of magnitude less than that required by structural collapsing for very large circuits. For a 1024-bit full adder, structural collapsing takes 39.9 seconds while hierarchical collapsing only takes 2.31 seconds.