

This seminar will feature the following four papers that will be presented at the IEEE North Atlantic Test Workshop, May 11-13, 2005.

IEEE P1500 compliant Modified Bidirectional Boundary Scan Cell for SoC testing

Nitin Yogi

The IEEE P1500 proposed system-on-chip (SoC) test standard facilitates embedded core testing and core test re-use. P1500 defines boundary scan cells (BSCs) for each terminal of the core for loading test vectors and capturing results. Bidirectional signals on cores are incompliant with P1500, and require modifications to be able to support the standard indirectly. Such modifications are not always possible, as in the case of legacy cores with bidirectional signals that cannot be modified. This paper suggests alternative architectures to the conventional BSC structures used to handle bidirectional signals. Bidirectional Boundary Scan structures using transmission gates and tri-state buffers are proposed, that can be directly interfaced to the bidirectional signals of the core. The proposed structures show an average reduction of 10 to 57% in the number of transistors for the BSCs, depending on the bus width, as compared to the indirect method of P1500 to support bidirectional signals.

On Embedded Processor Reconfiguration of Logic Built-In Self-Test for FPGA Cores in SoCs

John Sunwoo

The ability for an embedded processor core to reconfigure Field Programmable Gate Array (FPGA) cores in System-on-Chip (SoC) applications opens a number of new opportunities for Built-In Self-Test (BIST) of the FPGA cores themselves. The final paper will discuss some of the implications on BIST for FPGA cores using partial dynamic reconfiguration from an embedded processor including efficient ordering of the reconfiguration process, actual speed-up and memory savings associated with logic BIST, and the resulting affect on diagnosis of the FPGA.

Built-In Self-Test of Virtex and Spartan II FPGAs Using Partial Reconfiguration

Sachin Dhingra

Built-In Self-Test (BIST) of Field Programmable Gate Arrays (FPGAs) provides the ability of in-system testing without area or performance penalty to the intended system function. The primary problem is the long testing time and memory storage requirements associated with a large number of test configurations typically needed for complete testing of the programmable resources in the FPGA. Many recent FPGA architectures support the ability to reprogram only the portion of the FPGA that changes from one configuration to the next. This feature can be exploited to provide significant reductions in the amount of configuration data as well as the total testing time needed for testing of the FPGA.

Built-In Self-Test for I/O Buffers in ATMEL FPGAs

Sudheer Vemula

A Built-In Self-Test (BIST) approach is presented for the programmable Input/Output (I/O) buffers in Field Programmable Gate Arrays (FPGAs). The various modes of operation of the I/O buffers are tested along with their associated routing sources. A general BIST architecture, applicable to any FPGA, is presented along with the features and limitations of the approach. Specific BIST configurations were developed to test the I/O buffers in Atmel AT40K series FPGAs.