

# Practically Realizing Random Access Scan

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# Overview

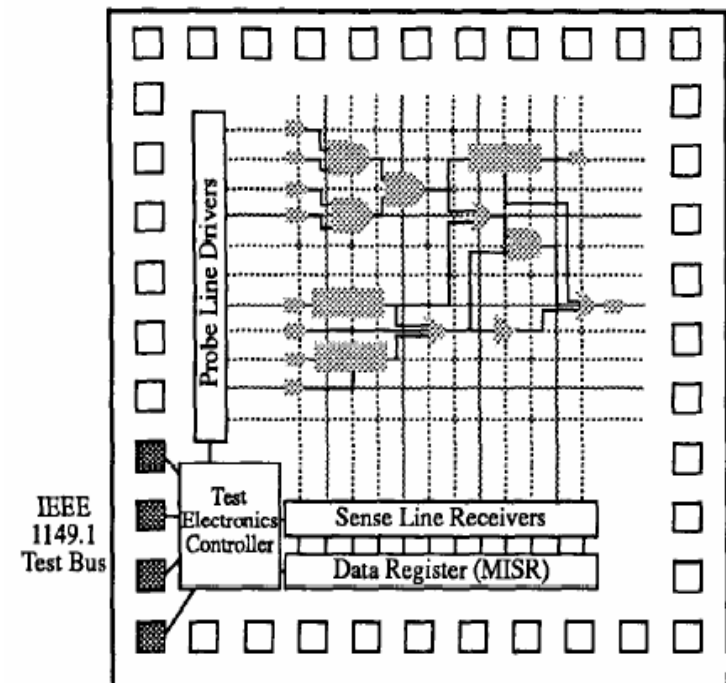
- Introduction to scan-based testing
  - Advantages
  - Limitations
- Solutions proposed and architecture implemented
- RAS routing
- Testing the test-circuit (monitoring the monitor)
- Compaction of test vectors
- Delay testing using RAS
- Further modification of ATPG to reduce test vectors
- Results
- Conclusion

# Serial Scan (SS)

- Enables application of combinational test vectors to sequential circuits
- Clock cycles prohibitive as number of FF increases
- Scan-in and Scan-out sequences result in unwanted circuit activity
- Test power reaches critical limit
- During every test, only a subset of all the FFs need to be set and observed for targeted faults

# Common methods to alleviate the limitations of SS

- Partial scan [AGRAWAL et al. 88]
  - Tradeoff between the ease of testing and the cost associated with scan.
- Cross check methodology [GHEEWALA et al. 91]
  - Provides comprehensive solution to test sequential circuits but area overhead is a limiting factor



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# Power issues of SS in more detail

- Power consumption during testing  $\gg$  normal circuit operation. Scan-in/Scan-out sequences trigger unnecessary circuit activity resulting in high power dissipation
- Vital and critical to target low power dissipation to avoid damaging the CUT

# Methods to alleviate the problem of excessive test power dissipation

- Test scheduling used in SOC [SALUJA et al. 91]
  - Test parallelism is reduced and test time eventually increases
- Scan clock is slowed down [CHANDRA et al. 94]
  - Again test application time increases
- ATPG based methods have been suggested [WANG et al. 01]
  - This often results in lengthy test sequences

# Methods to alleviate the problem of excessive test power dissipation

- Compaction of test vectors is often employed in testing. This generally results in increased circuit activity resulting in higher power consumption [TOUBA et al. 00]
- Test vectors for power saving have also been addressed [KAJAHARA et al. 02]
- Modification of the order of scan cells or inserting inversion logic between scan cells after the test generation [DABHOLKAR et al. 98]

# Random Access Scan (RAS)

- Concurrent solution to most of the problems in SS testing
- Each scan-cell is randomly and uniquely addressable
- Reduces both test application time as well as test power consumption, simultaneously, which are otherwise complementary objectives

# RAS Architecture

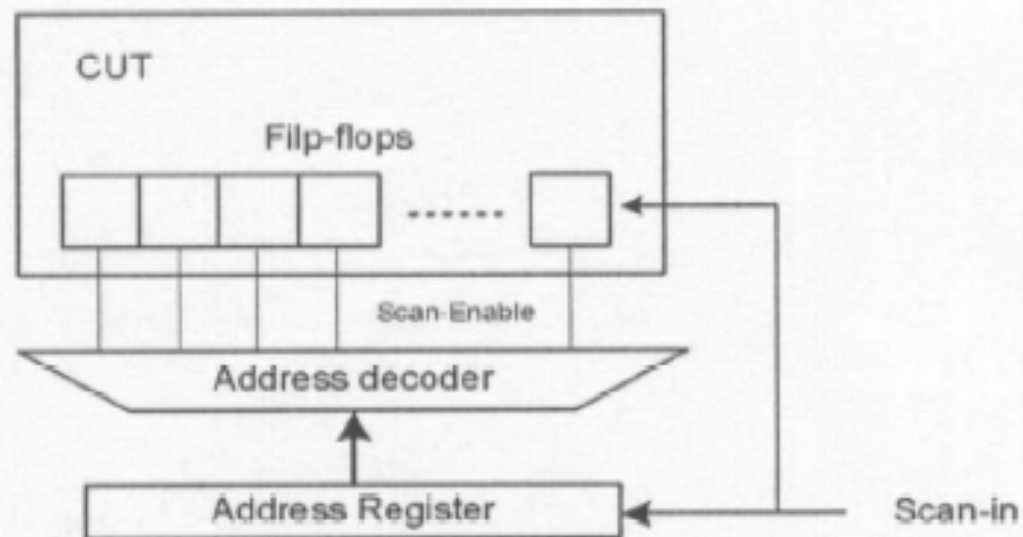
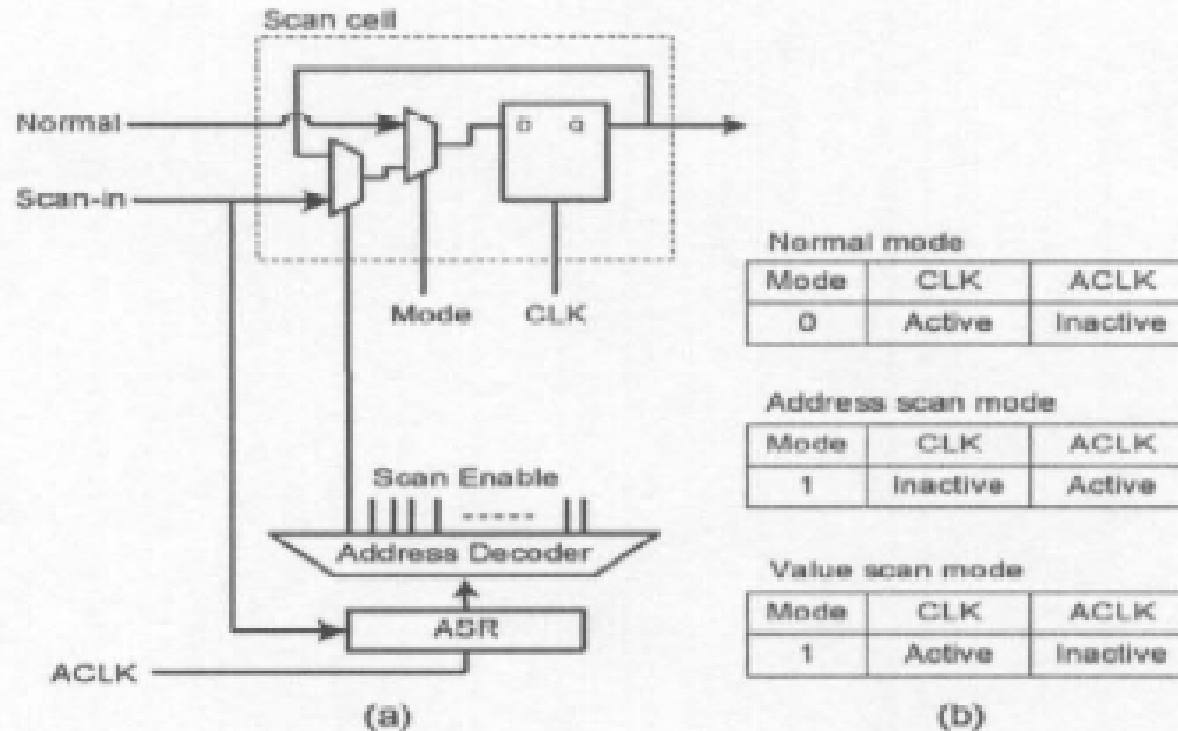


Figure 1: Abstracted structure of RAS

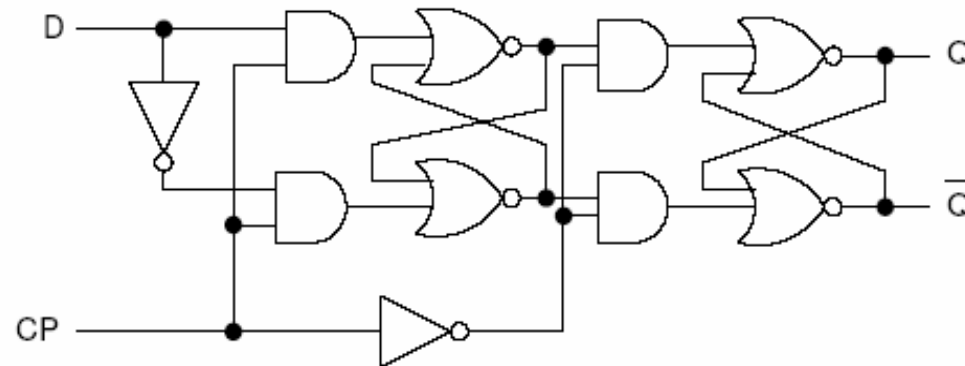
[SALUJA et al 04]

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# RAS Architecture



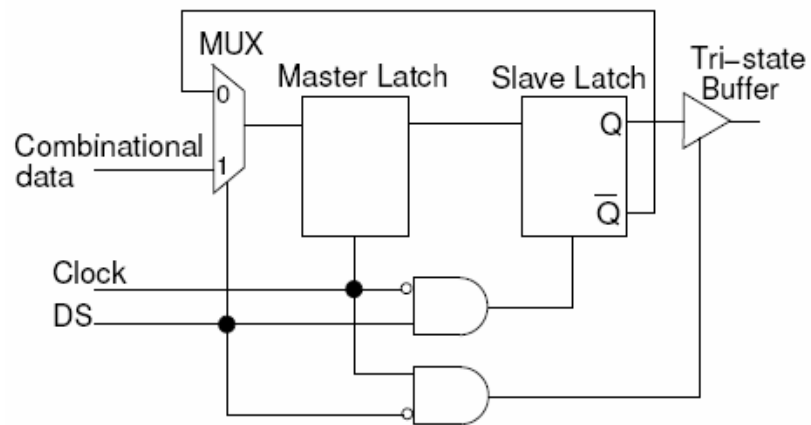
## RAS Architecture (cont.)



Master-Slave Latch

$Q = D$  at the end of a clock transition.

# RAS Architecture (cont.)

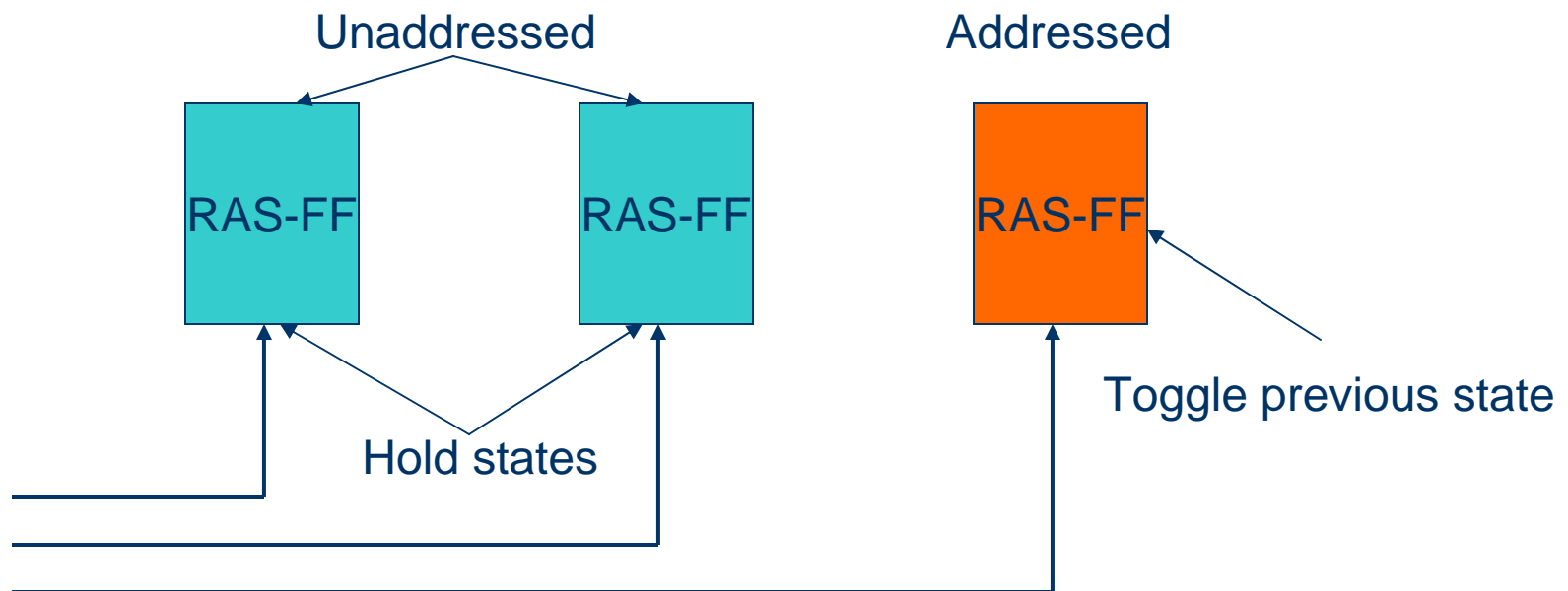


RAS-FF

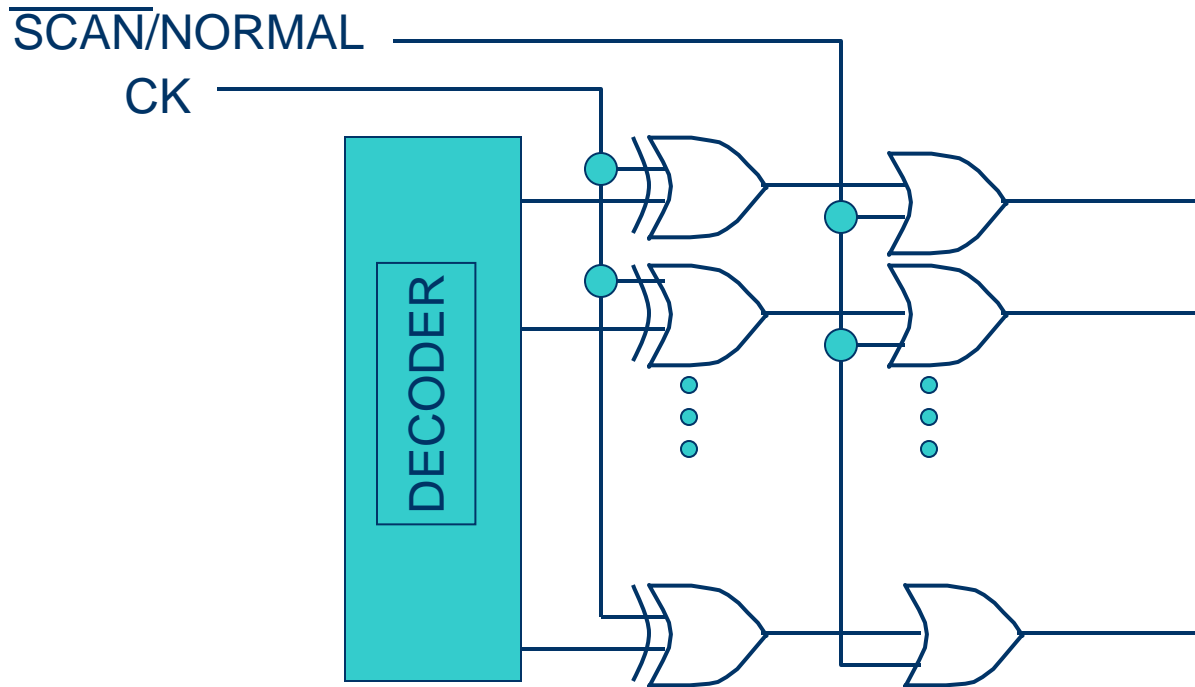
Function	CLOCK	Decoder Select (DS)
Normal data	1	1
	0	1
Toggle data	1	0
	0	1
Hold data	1	1
	0	0

signal sequence

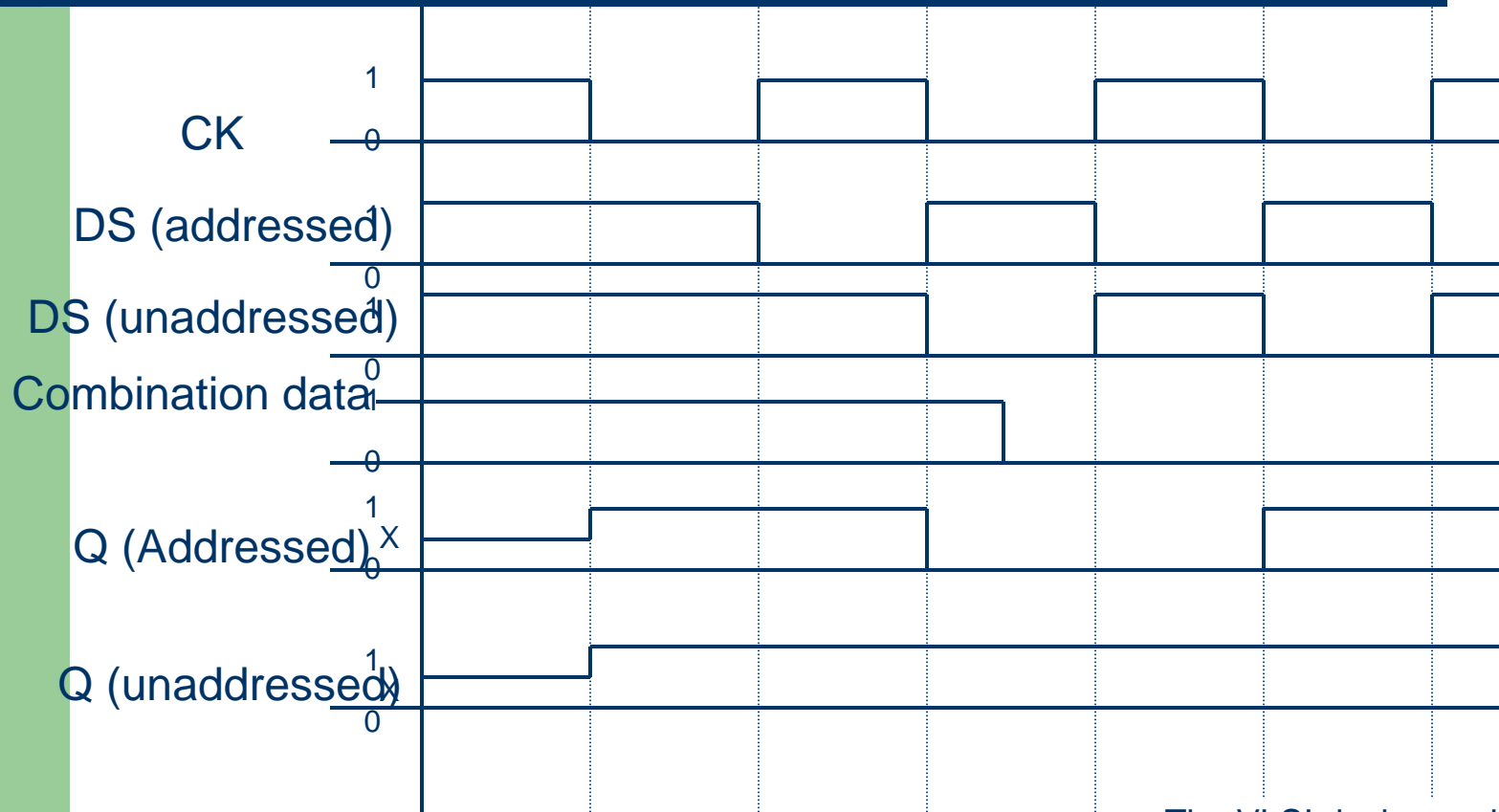
# RAS Architecture (cont.)



# RAS Architecture (cont.)



# RAS Architecture (cont.)



# Area overhead

- Gate overhead of SS =  $\frac{4 \times n_{ff} \times 100\%}{(n_g + 10 \times n_{ff})}$
- Gate overhead of RAS =  $\frac{7 \times n_{ff} \times 100\%}{(n_g + 10 \times n_{ff})}$

$n_{ff}$  = number of FFs

$n_g$  = number of gates

# Gate Area Overhead of RAS

Considering s38584 circuit,

No. of FF = 1426

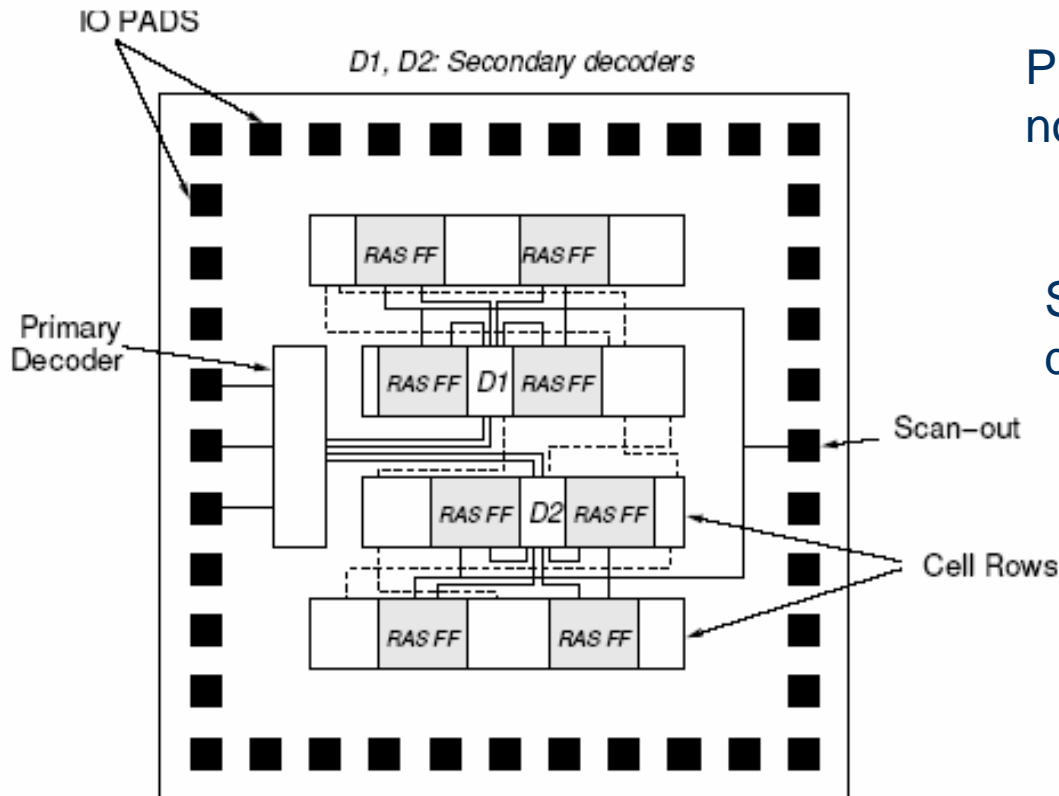
Total number of gates = 19253

Increase in no. of Gates in SS = 5704

No. of Gates in RAS = 9982

%increase in gates = 12.7%

# Routing




Primary Decoder: to decode non localized signals

Secondary Decoder: to decode localized signals

## Testing the RAS cell

- The decoder is first tested using the MATS++[19] test. The FFs are cleared initially since it is assumed that a clear operation is possible on all the FFs to initialize them and then the test is performed.

{  (w0);  (r0,w1);  (r1,w0,r0) }

 Addressing order can be either increasing or decreasing

 Increasing memory addressing memory order

 Decreasing memory addressing memory order

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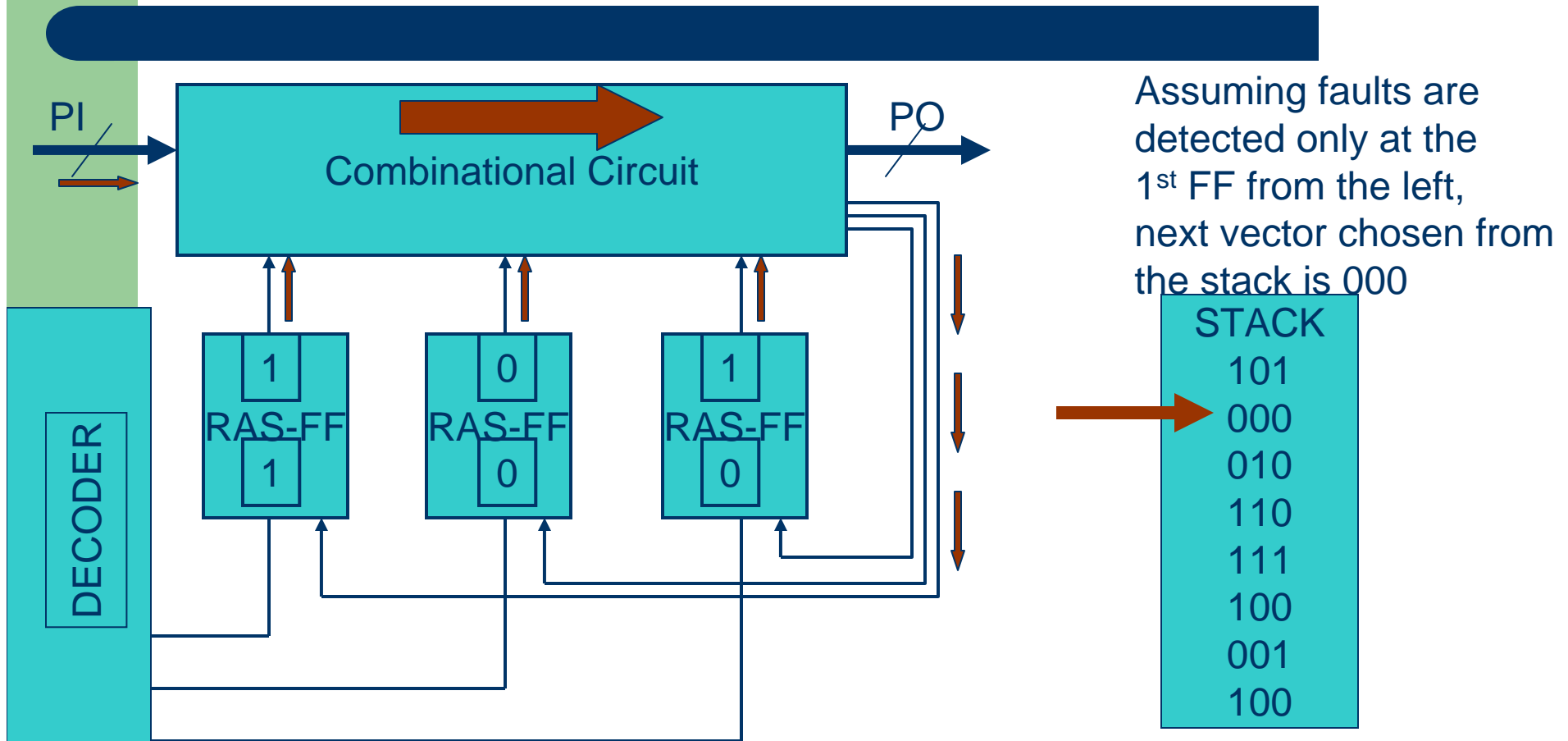
## Testing the RAS cell

- After the test-circuitry is tested for fault free operation, the FFs are set up to perform the routine tests
- The initial states are loaded into the FFs and the combinational inputs are applied at the primary input
- The vector sequences required to test the decoder and FFs, is **linearly proportional to the number of FFs in the circuit.**

# Algorithm to compact test vectors

- 1. Obtain the combinational vectors along with good circuit responses and store the results in a stack
- 2. Find the FFs where faults are propagated at each vector
- 3. While number of vectors  $> 0$ 
  - (a) Read all the FF where the faults are detected
  - (b) Choose the next vector from stack that has least hamming distance from current FF states
- 4. End While

# Compaction of test vectors

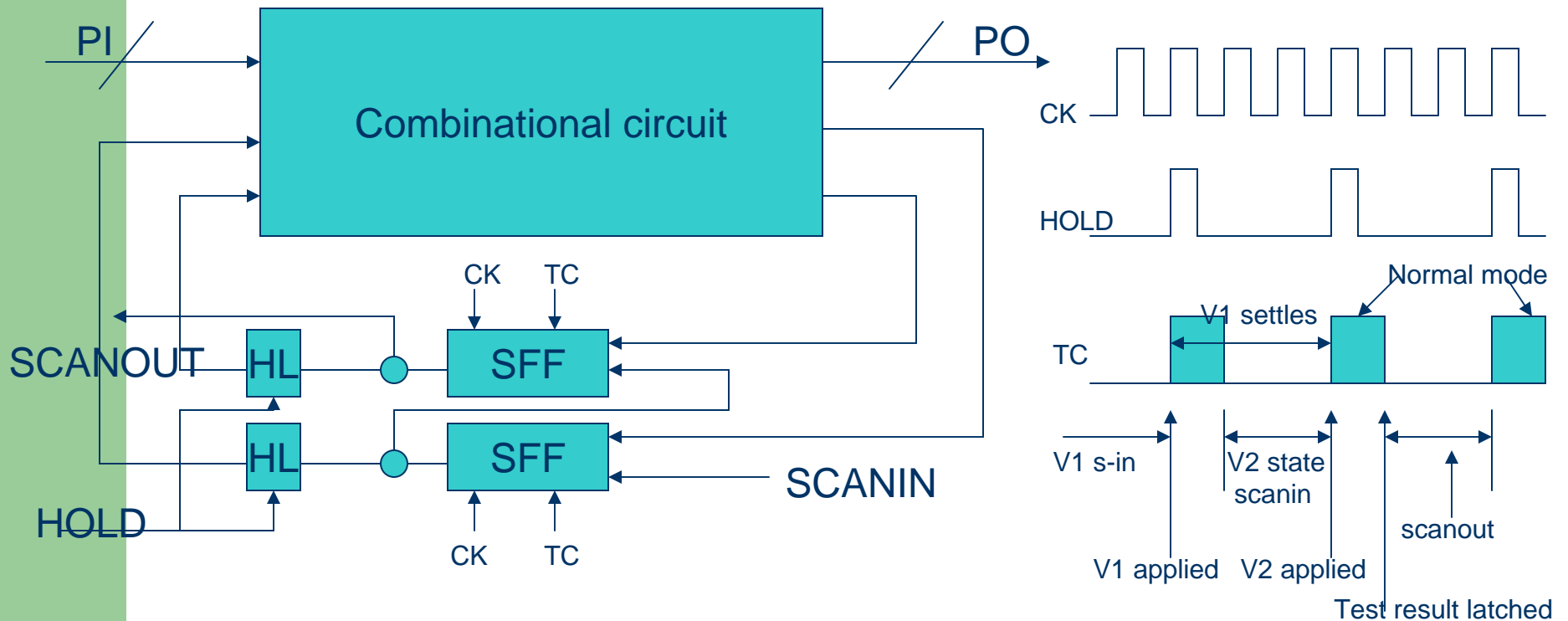


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# Delay testing using RAS

- Testing for path delay faults in non-scan sequential circuits is complicated by the limited state transitions during normal operation
- Delay testing in SS is very constrained
- An accepted method for overcoming this difficulty is to use a scan-chain consisting of enhanced scan FF which makes the application of arbitrary vectors possible
- However this technique requires a hold-latch connected to each FF in addition to a “HOLD” signal that must be routed to every hold latch
- Resulting in increased area overhead and some finite increase in signal delay in the scan path

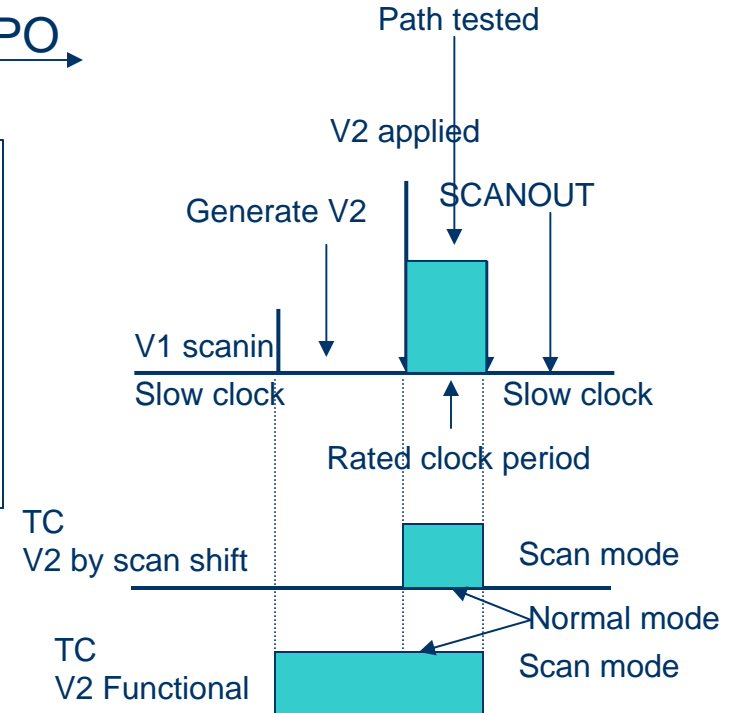
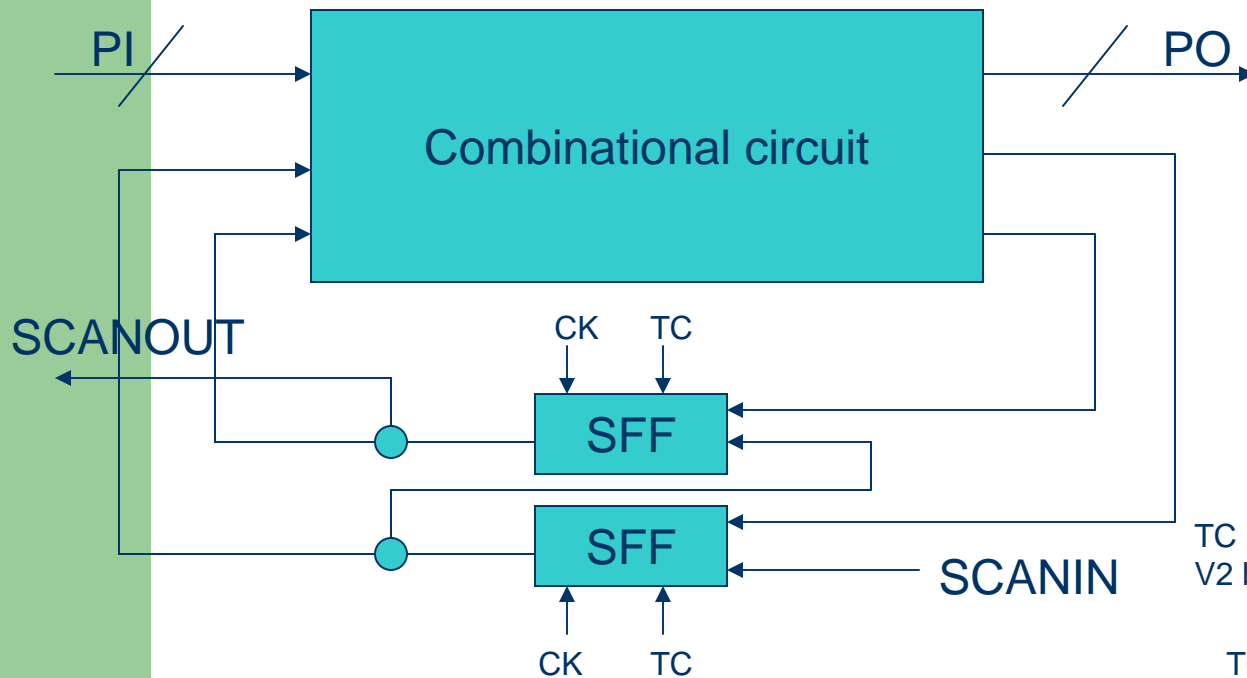
# Enhanced-scan delay test application to sequential circuit



## Delay testing using RAS (cont.)

- Normal scan sequential circuits can be tested for delay faults, but the vector-pairs must be specially generated
- The first vector is scanned in (usually with a slow scan clock) and is then replaced in the scan register by either
  - (a) applying V2 which is obtained by a one bit shift to the scan register also known as **scan-shift delay test**
  - (b) propagating V1 through the combinational logic in the normal mode, where the state portion of V2 may be justified by V1, known as **functional broad-side delay test**
- Fault coverage depends on the circuit and cannot be guaranteed due to the correlation between the two vectors

# Normal-scan delay test application to sequential circuit



## Delay testing using RAS (cont.)

- Normally a one bit change is desired while targeting a delay fault
- In RAS vector V1 is setup and vector V2 can be subsequently applied without any constraints since, any FF can be arbitrarily addressed and the response can be captured during the next clock
- This completely solves the problem of choosing special vectors to be generated for delay testing
- Hence any pair of vectors with a one bit change can be used in RAS without additional hardware

# Results

- The architecture was implemented on ISCAS benchmark circuits and the fault coverage were the same as that of serial scan
- A reduction of up to 60% can be observed just by modifying the existing ATPGs
- Maximum reduction is achieved when the average number of faults detected per combinational vector is small and the number of FFs is proportionally higher. Since in these cases the setup time of scan FFs would increase compared to RAS.

Circuit	No. of FFs	No. of Combi. vectors	No. of SS vectors	No. of RAS vectors	Test time red. (%)
s27	3	12	51	28	45.1
s208	8	64	584	301	48.46
s349	11	42	687	366	46.72
s386	6	138	972	450	53.70
s420	16	128	2192	1056	51.82
s510	6	110	776	344	55.67
s641	19	142	2859	1148	59.85
s838	32	240	7952	3595	54.79
s1196	18	344	6554	2447	62.66
s1269	37	118	4521	1981	56.18
s3271	116	264	31004	12540	59.55
s3384	183	260	48759	21119	56.69
s5378	179	618	111419	48677	56.31
s13207	638	1138	727820	309132	57.53

## Results (cont.)

- Relative reduction of power dissipation in the circuit is calculated assuming that, the power dissipated is directly proportional to the number of transitions in the primary inputs and states of FFs. [Devadas et al. 95]
- The results were obtained for both SS and RAS
- It can be observed that, as the size of the circuits increases, reduction in power dissipation upto 99% is achieved using RAS.

Circuit	No. of Transitions in SS tests	No. of Transitions in RAS tests	Test power saving (%)
s27	94	72	23.4
s208	1866	1209	35.21
s349	4755	1233	74.07
s386	2495	1515	39.28
s420	11587	4708	59.37
s510	3141	2382	24.16
s641	27715	7924	71.41
s838	72914	17782	75.61
s1196	57409	10601	81.53
s1269	77755	7880	89.87
s3271	1744149	45971	97.36
s3384	4299362	77665	98.19
s5378	8947677	175710	98.04
s13207	230176409	211048	99.91

# Modifications in ATPG to further decrease the number of vectors

- A slight modification in the form of an added constrain in the ATPG, can further decrease the test vectors using RAS.

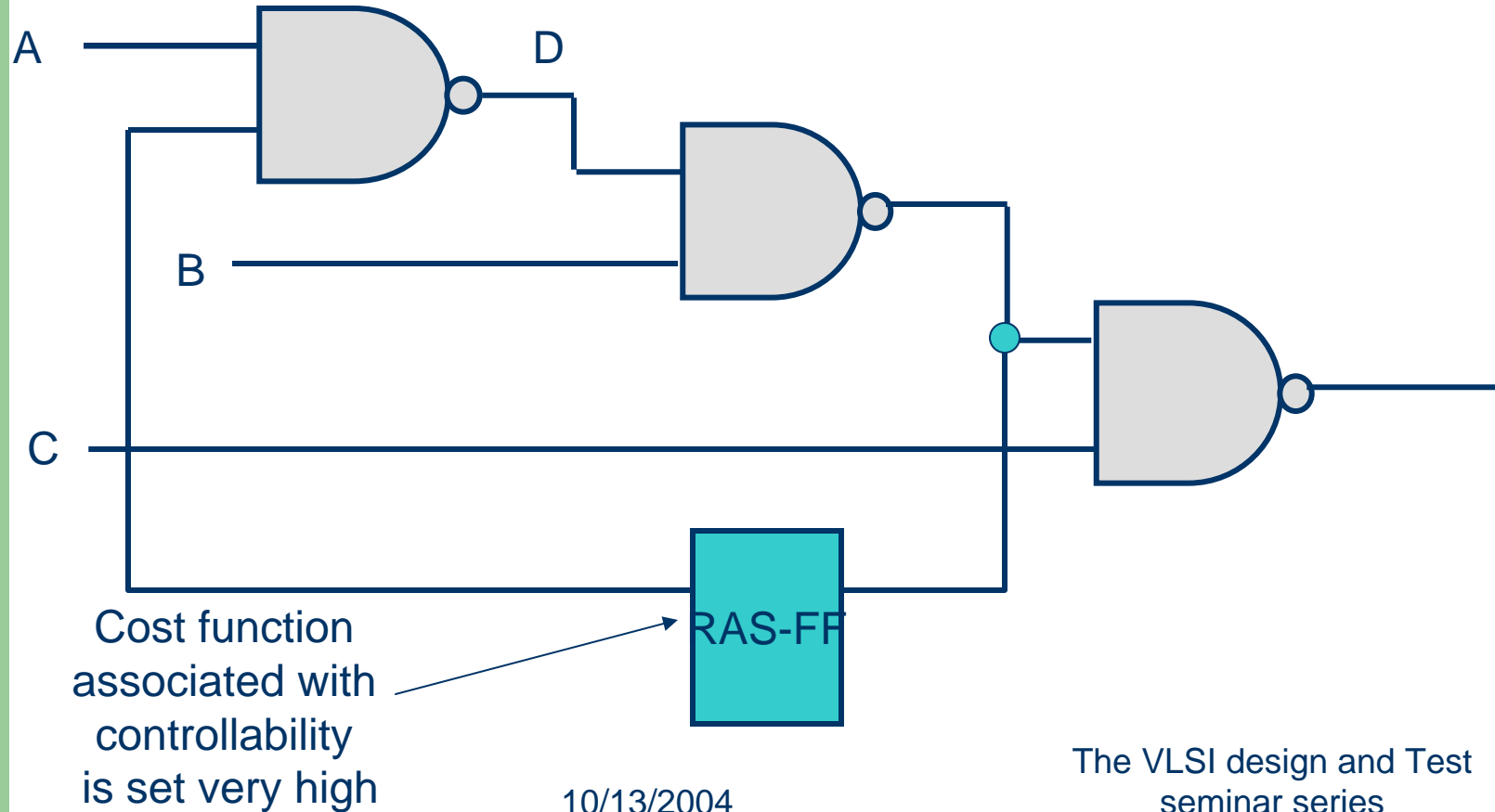
## Algorithm:

1. Set the cost function of setting a FF to be highest
2. Generate a vector to target a fault
3. Perform Fault simulation
4. While number of faults  $> 0$ 
  - (a) Read all the FF where the faults are detected
  - (b) Target a fault and Generate the next vector with minimum changes to be made in the FFs from the current states.
  - (c) Perform Fault simulation
5. End While

## Modifications in ATPG to further decrease the number of vectors (cont.)

- Let us consider modifying PODEM's backtrace algorithm, where the pseudo-controllability of the FF (pseudo primary inputs) is set very high
- Hence during backtrace, minimal set of FFs are set for a targeted fault
- This algorithm was implemented on s27 circuit, in which 12 vectors were generated by the combinational ATPG, and applying the constraints of the algorithm resulted in 16 vectors which is a reduction of 43% compared to the results obtained when a vector reordering scheme was used earlier and 68% decrease against the number of scan vectors.
- It is intuitive that, better vector compaction can be achieved for larger circuits using this algorithm.

# Modification of PODEM's Backtrace algorithm



# Conclusion

- Skepticism towards RAS in the past have mainly been due to the excessive area overhead in the form of routing and suggested architectures
- RAS is an ideal solution to target test volume and test power which are otherwise complementary
- Efficiently laying out the circuit and deploying the decoders optimally would keep the area overhead to a minimum
- This work is based on the premise that as technology advances (more gates per die), a minimal increase in design for testability (DFT) at the cost of reduced computational resources and increased flexibility in testing, will be least prohibitive.

# Topics for further exploration

- Optimizing routing overhead, carefully choosing the location of the decoders
- Delay testing
- RAS using BIST

