VLSI/FPGA Design and Test CAD Tool Flow in Mentor Graphics

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or....
"Nightmare on
CAD Tool Street"

Mentor Graphics CAD Tool Suites

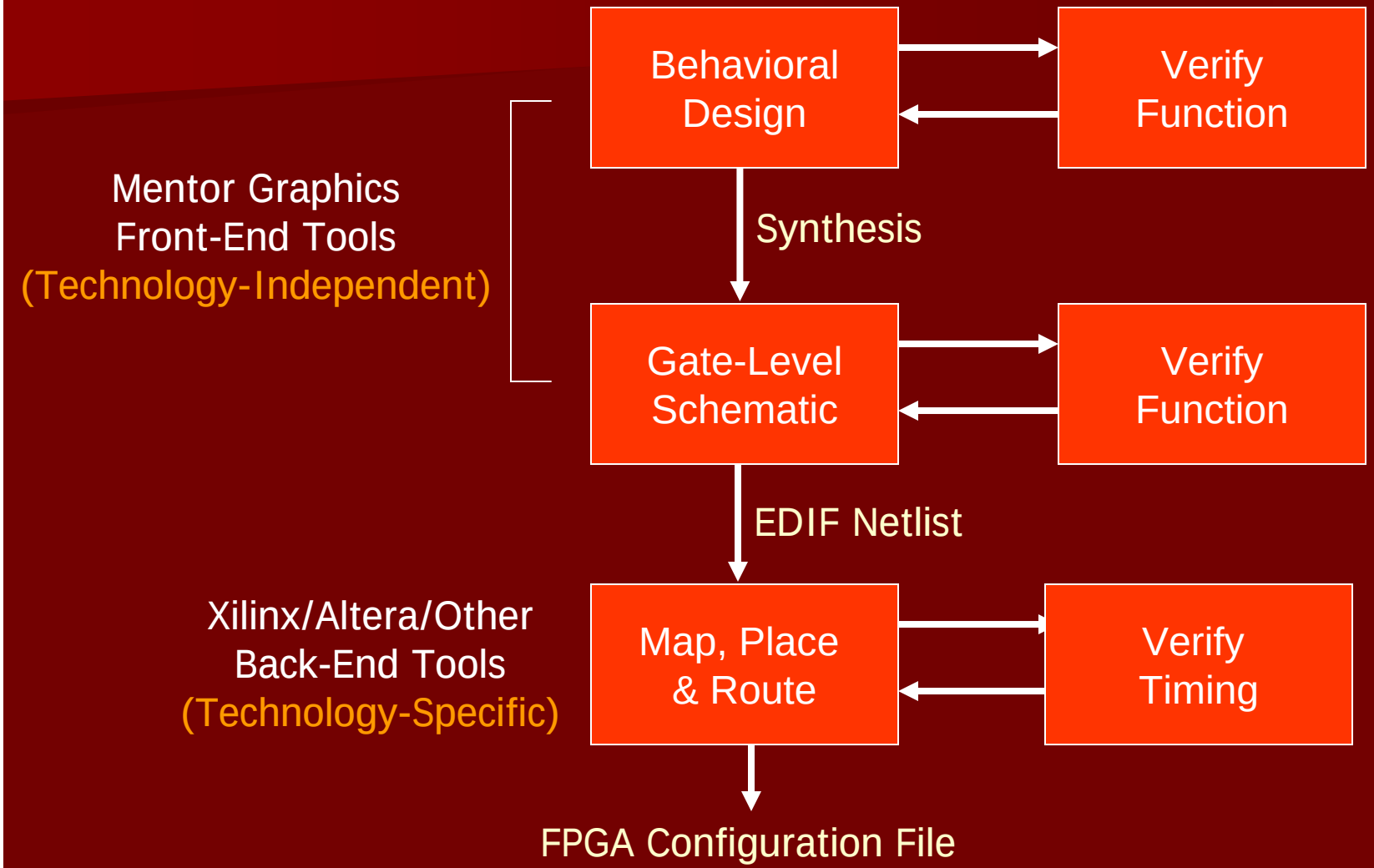
- IC/SoC design flow
- DFT design flow
- FPGA design flow
- PCB design flow
- HDL digital modeling & simulation
- Analog/mixed-signal modeling & simulation
- ASIC/FPGA synthesis

- Vendor-provided (Xilinx,Altera,etc.) back end tools

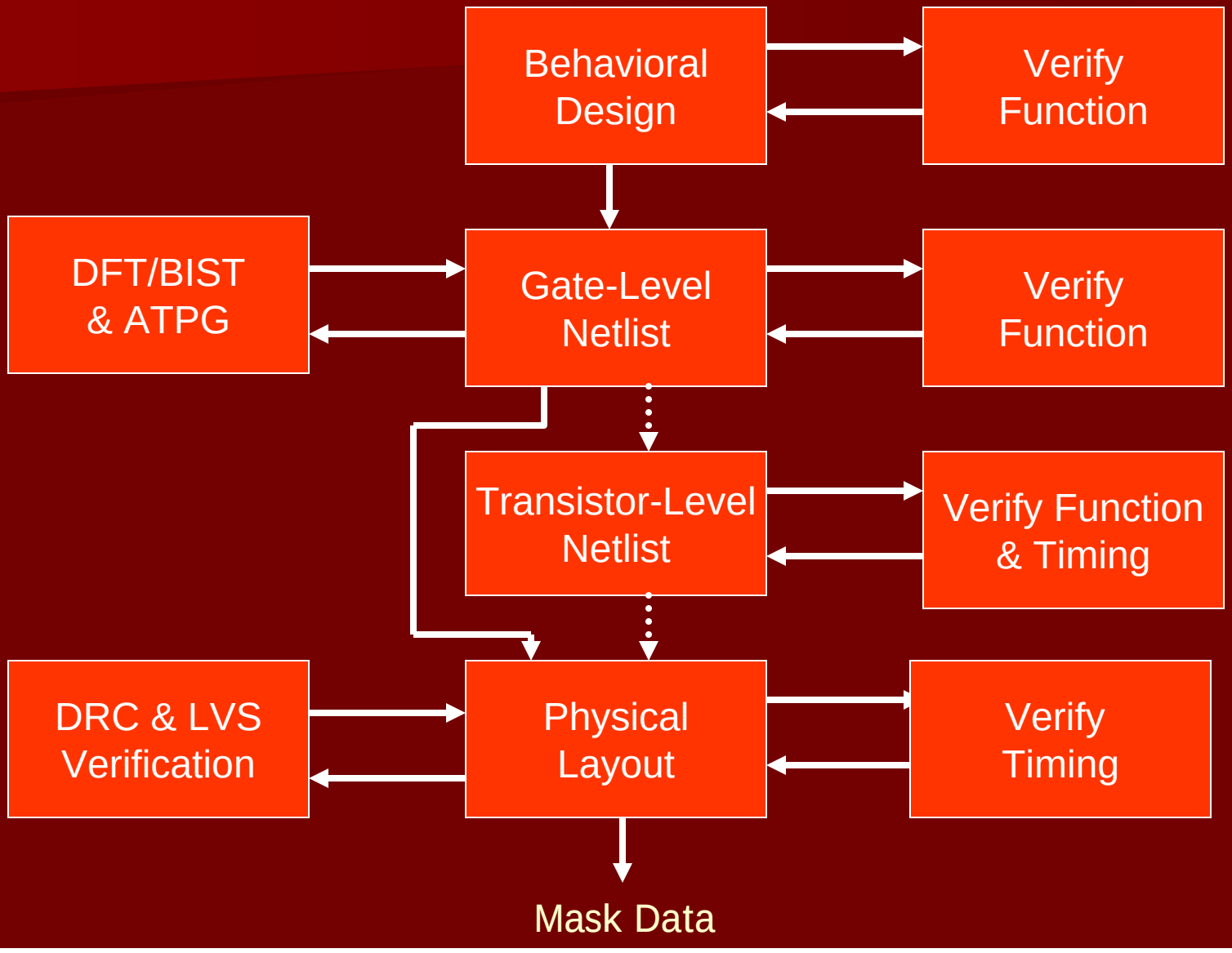
Auburn “user-setup” Options
(select “eda” – Electronic Design Automation)

- ICFlow2004.3 *(2001, 2005.1)*
  - ICFlow tools *(Design Architect-IC, IC Station, Calibre)*
  - Simulation tools *(Modelsim, ADVance MS, Eldo)*
  - Synthesis *(Leonardo)*
  - DFT tools *(DFT Advisor, Flextest, Fastscan)*
  - Limited access to Quicksim II *(some technologies)*
- EN2002u3 *(EN2001)*
  - Design Architect, Quicksim II,Quicksim Pro *(Front End)*
  - ModelSim & Leonardo *(Simulation/Synthesis)*
  - Xilinx/Altera tools *(Back End)*
- FPGA *(FPGA Advantage, Modelsim, Leonardo)*

FPGA Design Flow



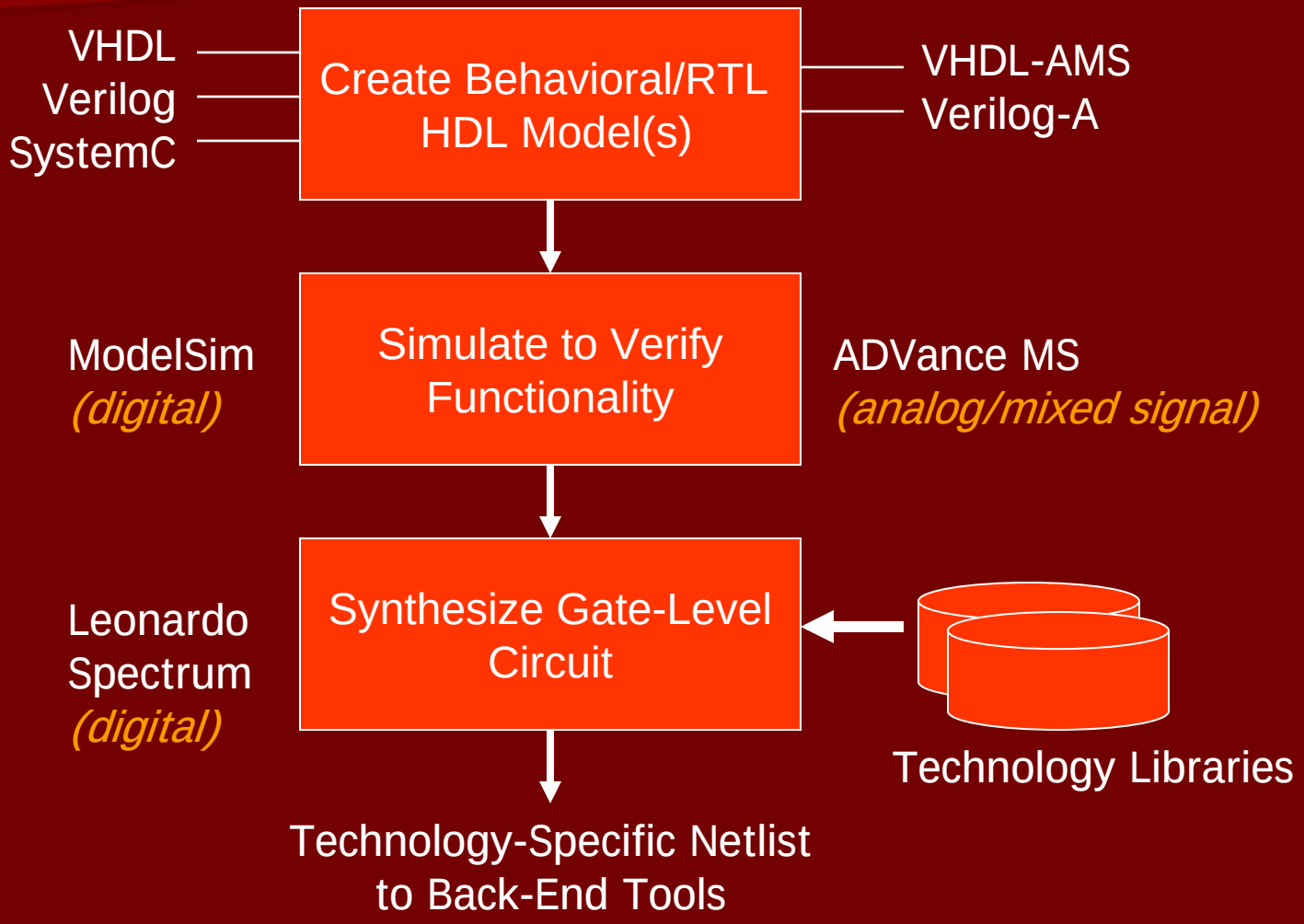
IC/ASIC Design Flow



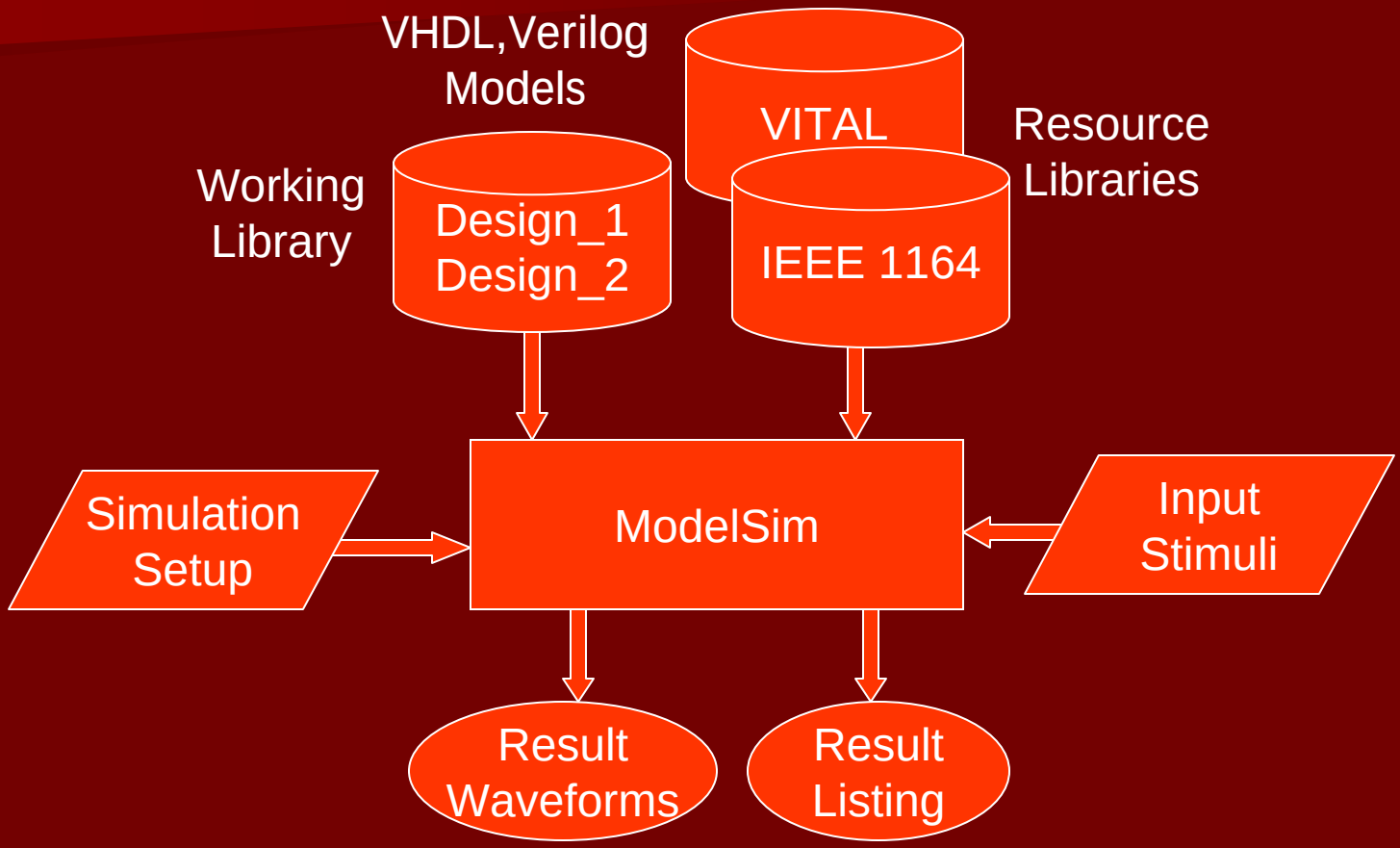
Mentor Graphics ASIC Design Kit 3.0

- Technology files (all) & standard cell libraries (exc. tsmc018)
  - ami12, ami05 (AMI 1.2um, 0.5um)
  - tsmc035, tsmc025, tsmc018 (TSMC 0.35um, 0.25um, 0.18um)
- Support for IC Flow & DFT tools:
  - Synthesis *(LeonardoSpectrum)*
  - Schematic capture *(Design Architect-IC)*
  - Design for test & ATPG *(DFT Advisor, Flextest/Fastscan)*
  - Simulation
    - *Modelsim/ADVance MS*: VHDL/Verilog/Mixed-Signal models
    - *Eldo/Accusim* analog (SPICE) models
    - *Mach TA* post-layout timing
    - *Quicksim II, Quicksim Pro* (except tsmc025,tsmc018)
  - IC layout & verification (standard cell & custom)
    - *IC Station*
    - *Calibre, SST Velocity*

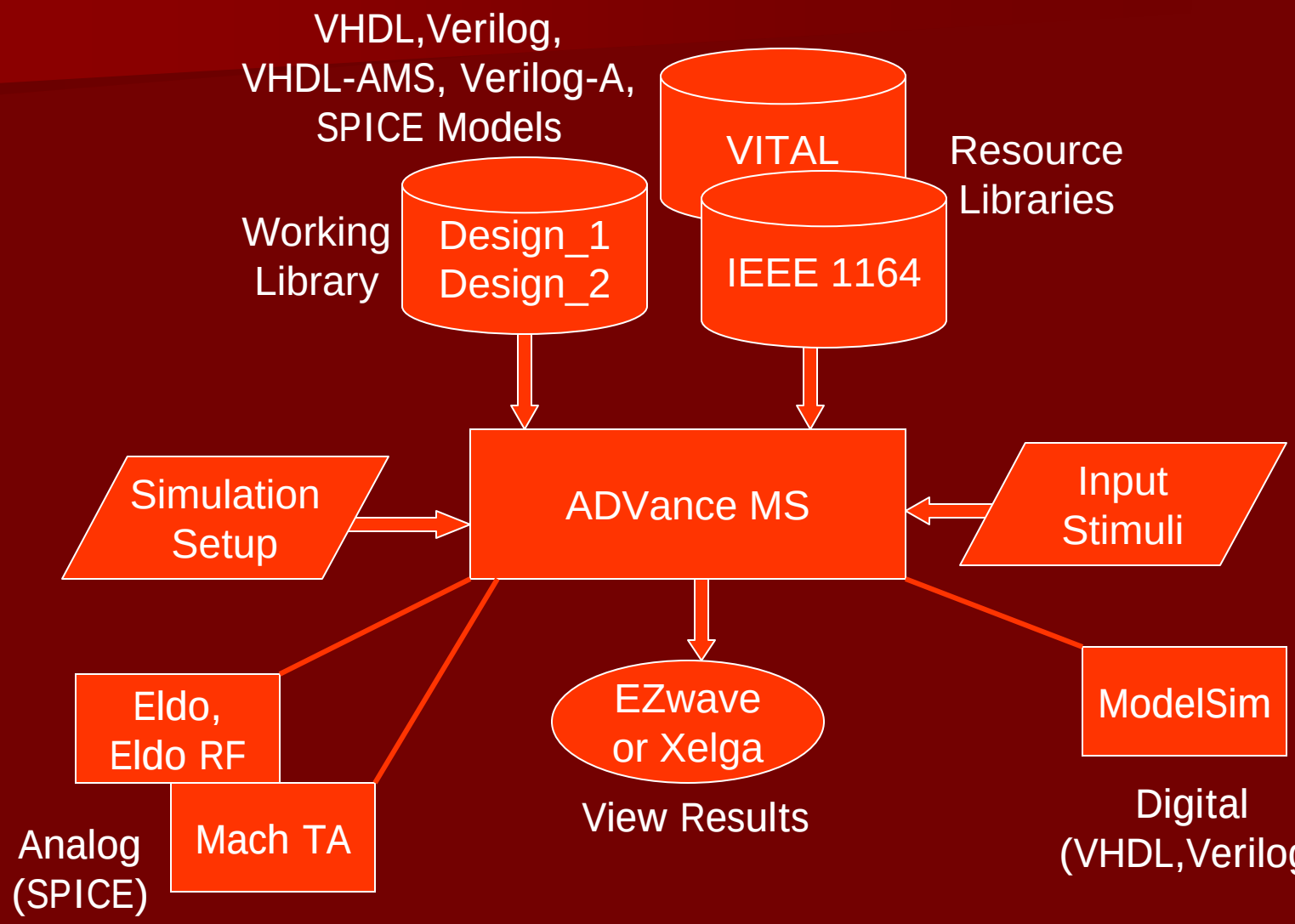
Behavioral Design & Verification
(mostly technology-independent)



Digital HDL Simulation



Mixed-Signal HDL Simulation

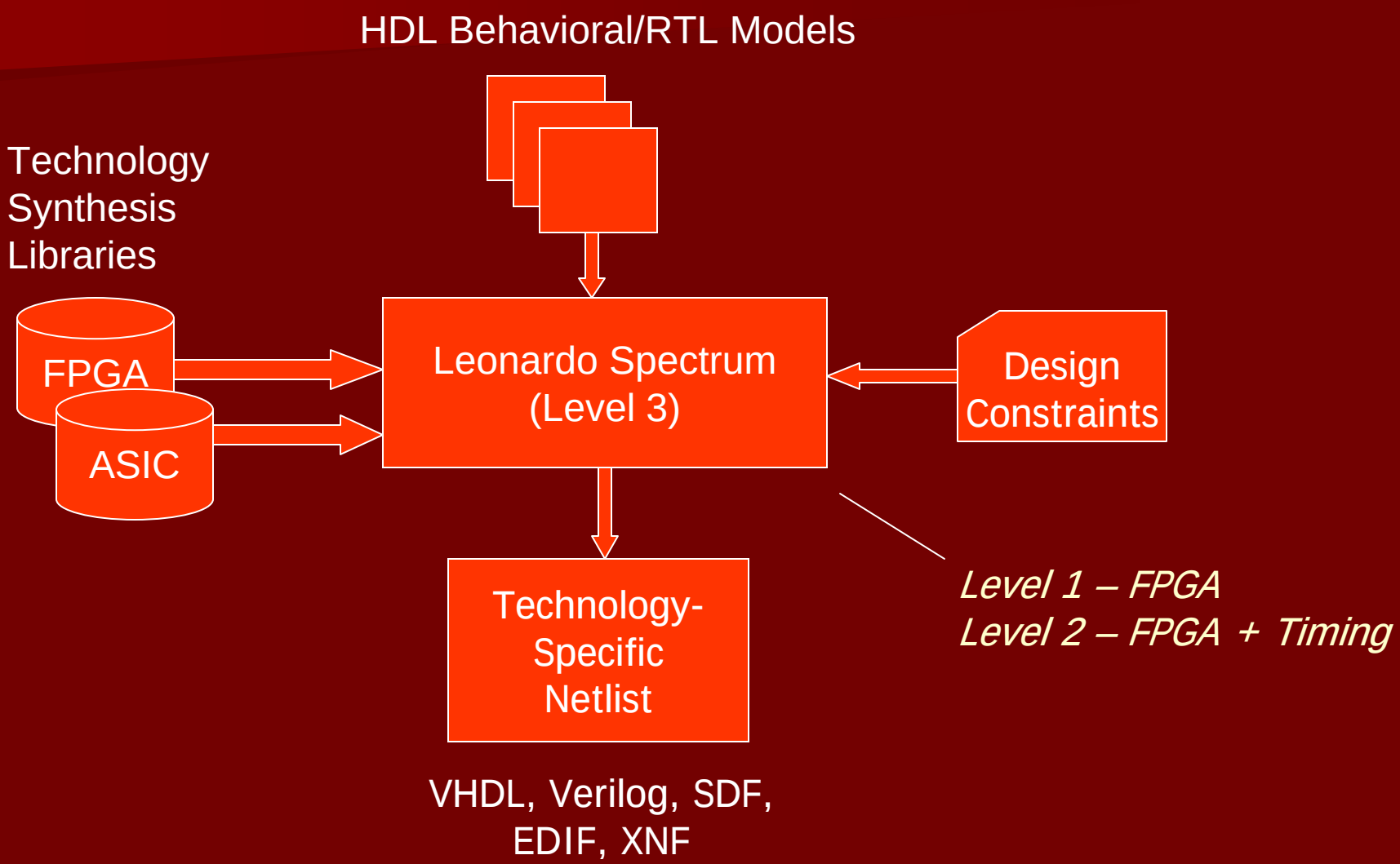


ADVance MS Simulation System

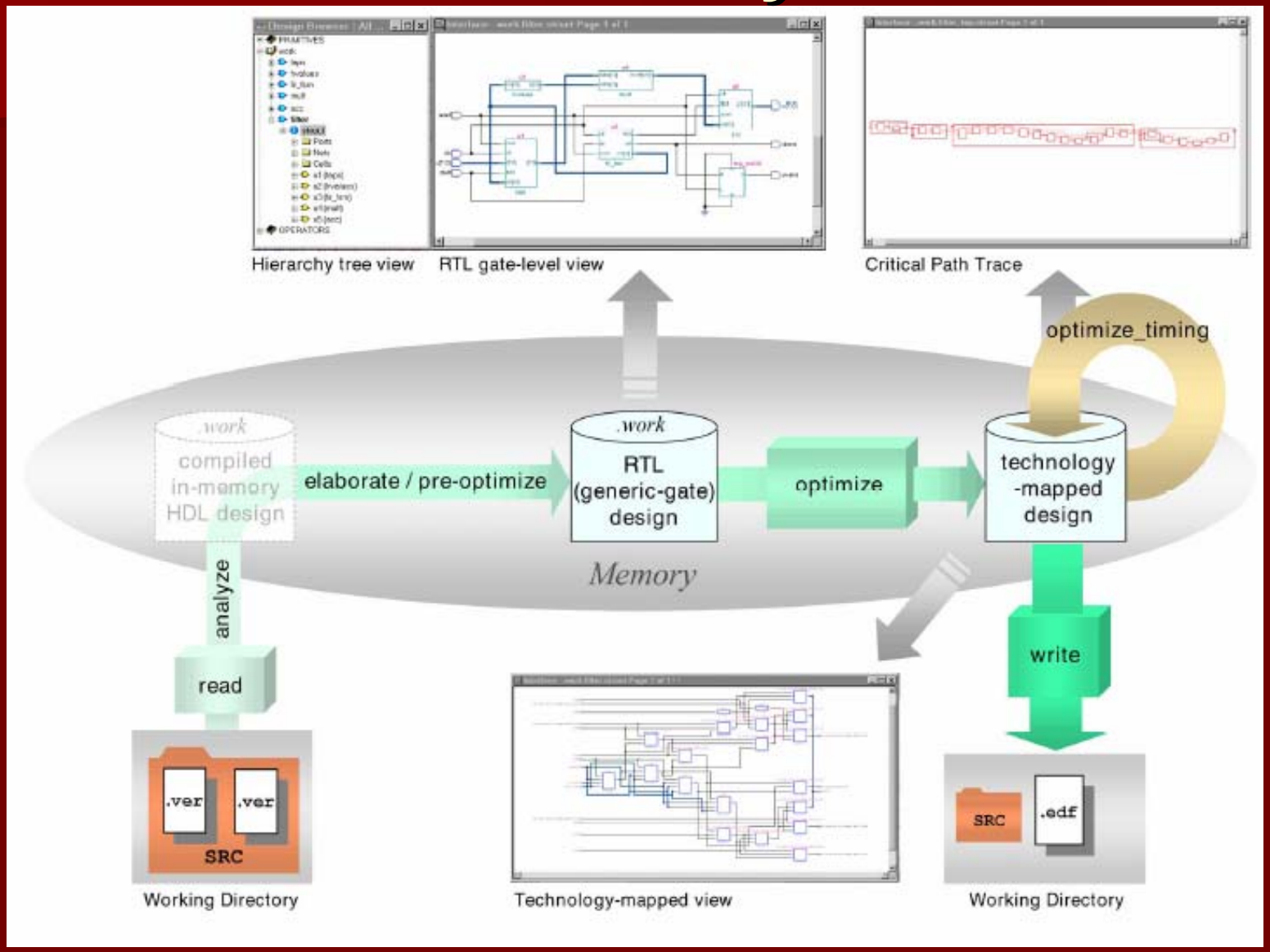
- ADVance MS “kernel” supports:
  - VHDL & Verilog: digital (via ModelSim)
  - VHDL-AMS & Verilog-A: analog/mixed signal
  - Eldo/SPICE: analog (via Eldo)
  - Eldo RF/SPICE: analog RF (via Eldo RF)
  - Mach TA/SPICE: high-speed analog/timing
- Invoke stand-alone or from Design Architect-IC

- Mentor Graphics “Legacy” Simulators (PCB design)
  - Quicksim II, Quicksim Pro (digital)
  - ASIC: *adk_quicksim*
  - FPGA/PLD: Xilinx: *pld_quicksim*, Altera: *max2_quicksim*
  - Accusim (analog): *adk_accusim*

Automated Synthesis



Leonardo – ASIC Synthesis Flow



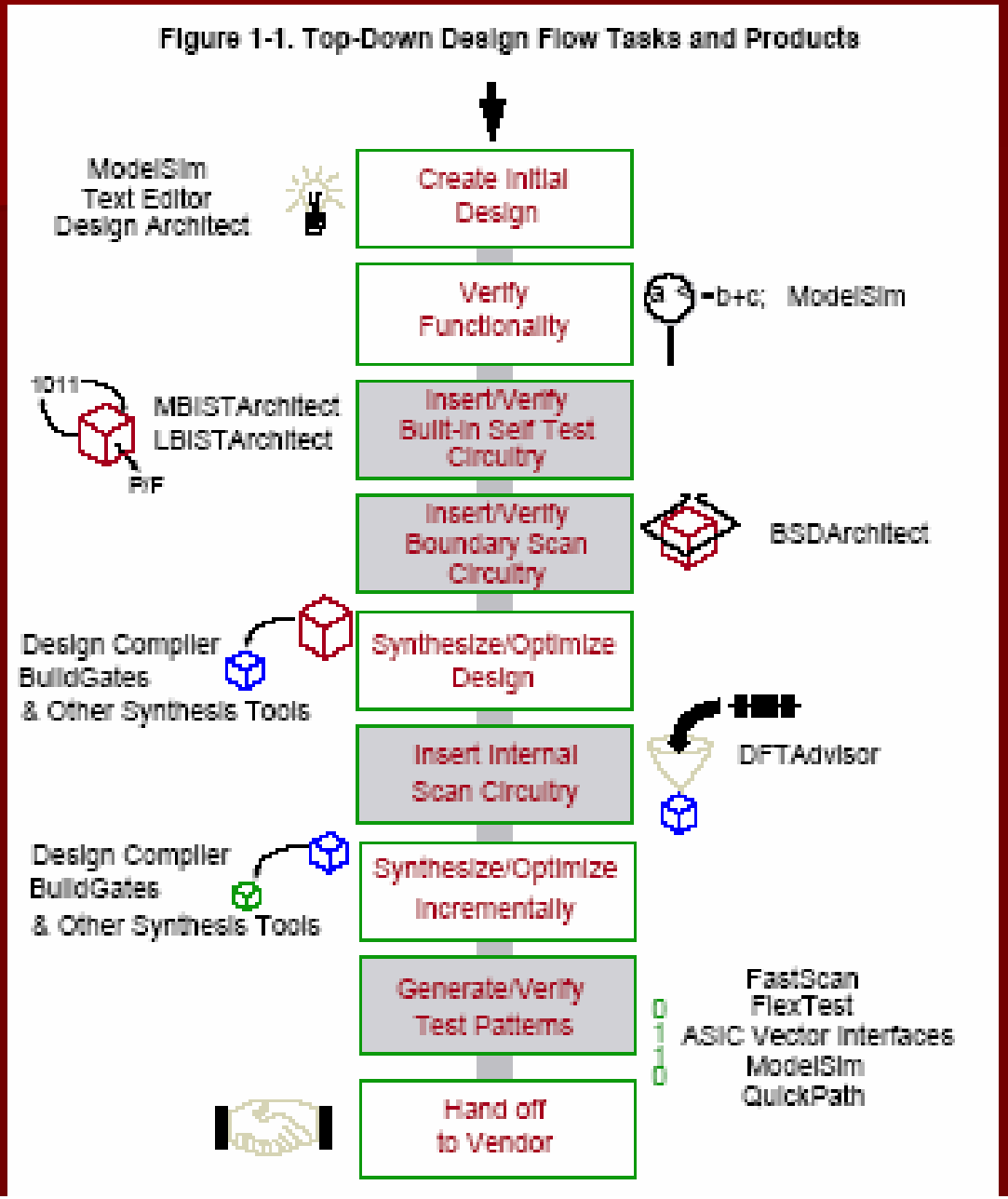
Synthesis Example

- Load technology library:

  tsmc035 (ASIC), or Xilinx Spartan2 (FPGA)
- Load design file: seqckt.vhd
- Specify constraints: clock freq, delays, etc.
- Optimization: effort, performance vs. area
- Write synthesized netlist output(s):
  - seqckt_0.vhd : VHDL netlist for ModelSim & DFT
  - seqckt.v : Verilog netlist for import into DA-IC
  - seqckt.sdf : For ModelSim to study timing
  - seqckt.edf : EDIF netlist for 3rd party tools
  - seqckt.xnf : Xilinx netlist for Xilinx ISE

Mentor Graphics DFT Design Flow

Memory & Logic BIST →

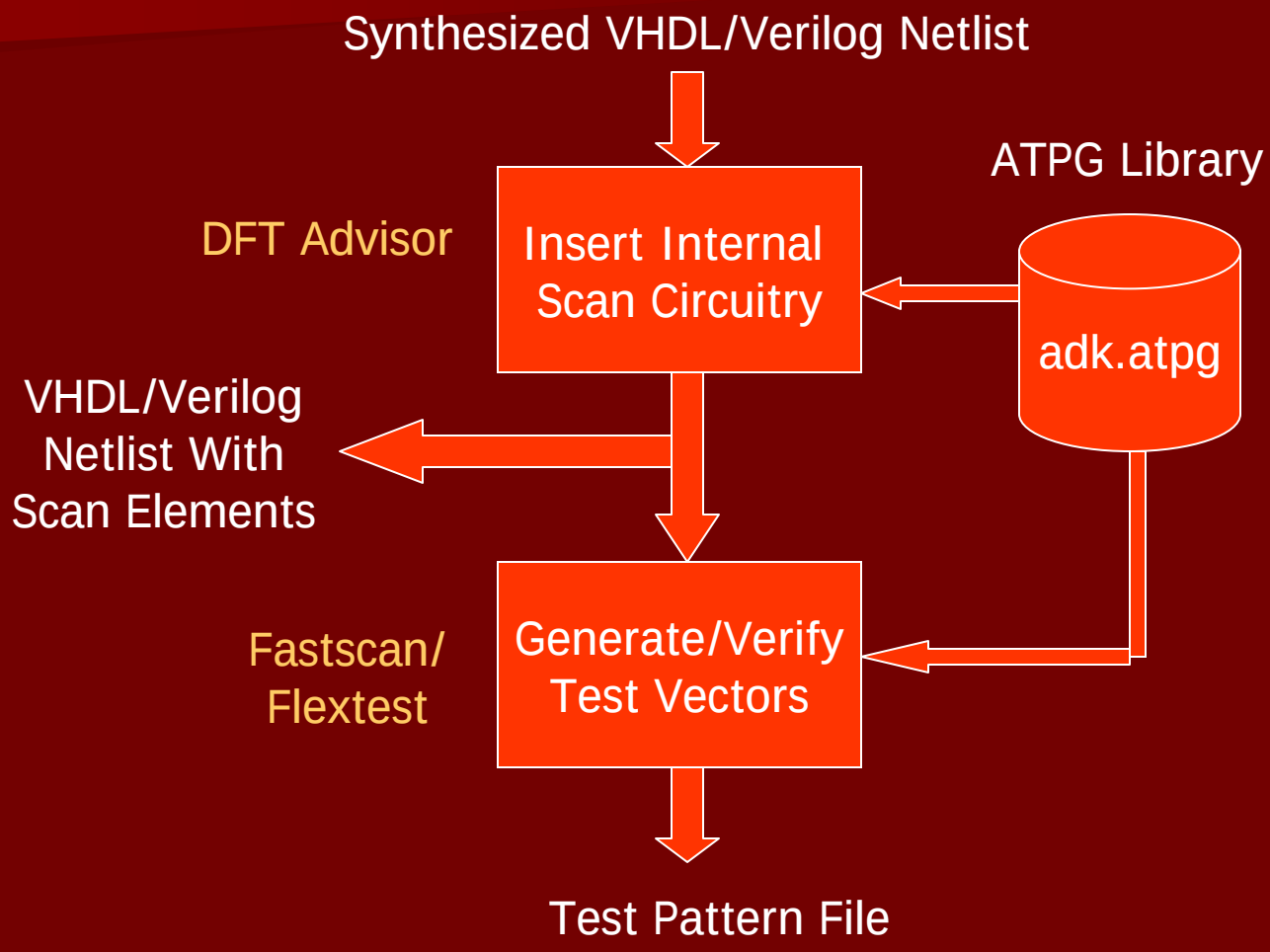


← Boundary Scan

← Internal Scan Design

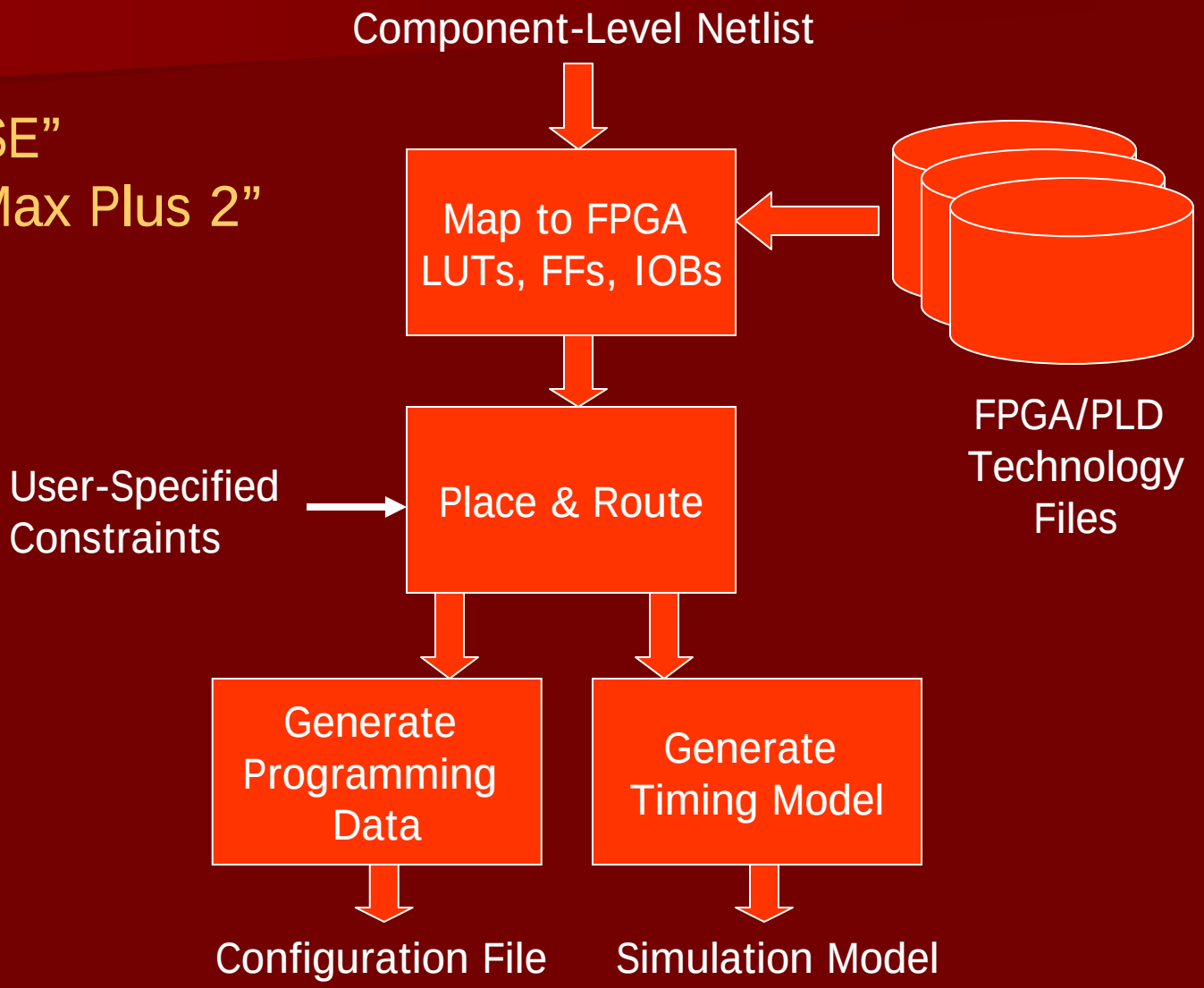
← ATPG

ASIC DFT Flow

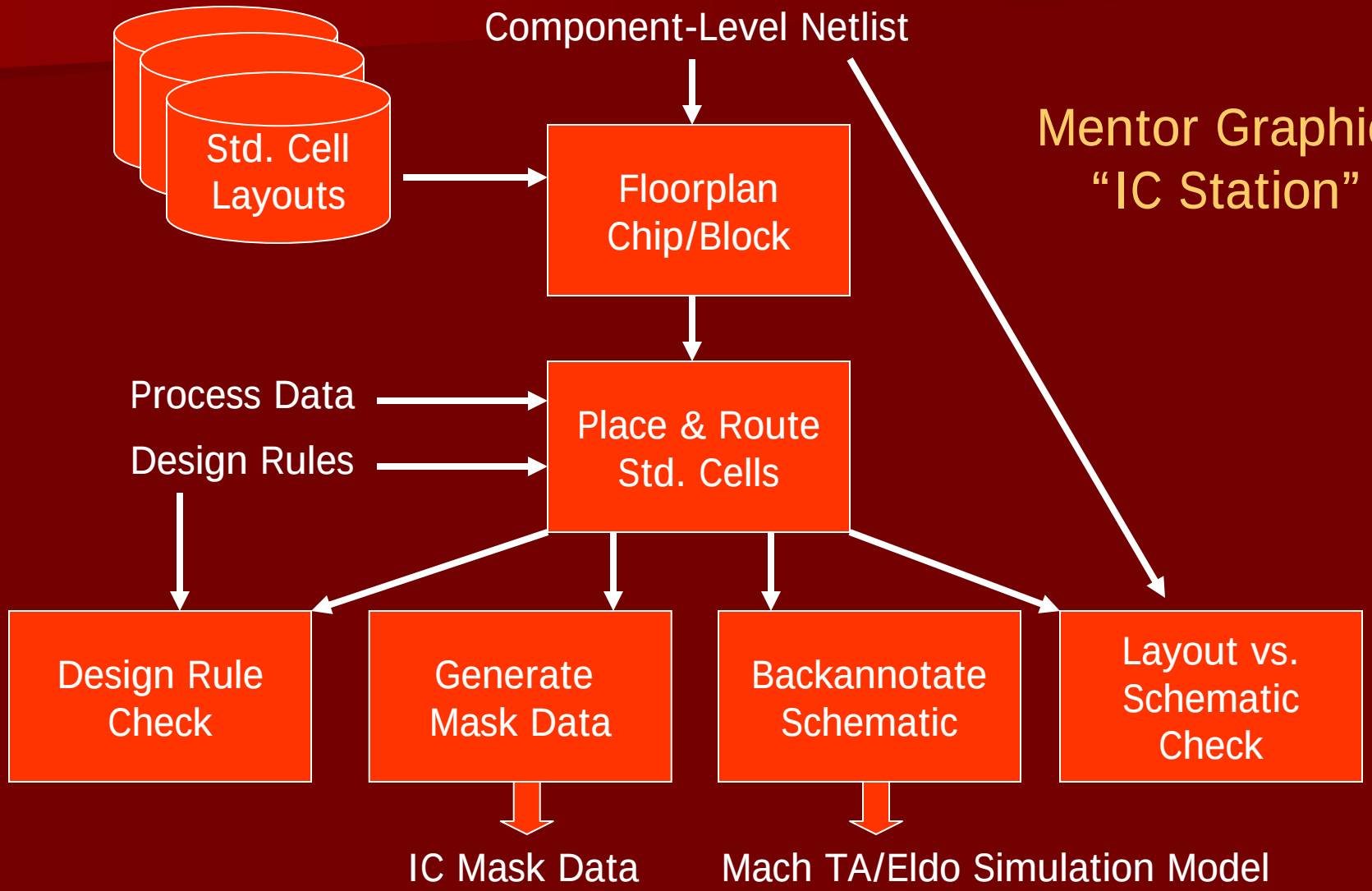


Physical Design - FPGA

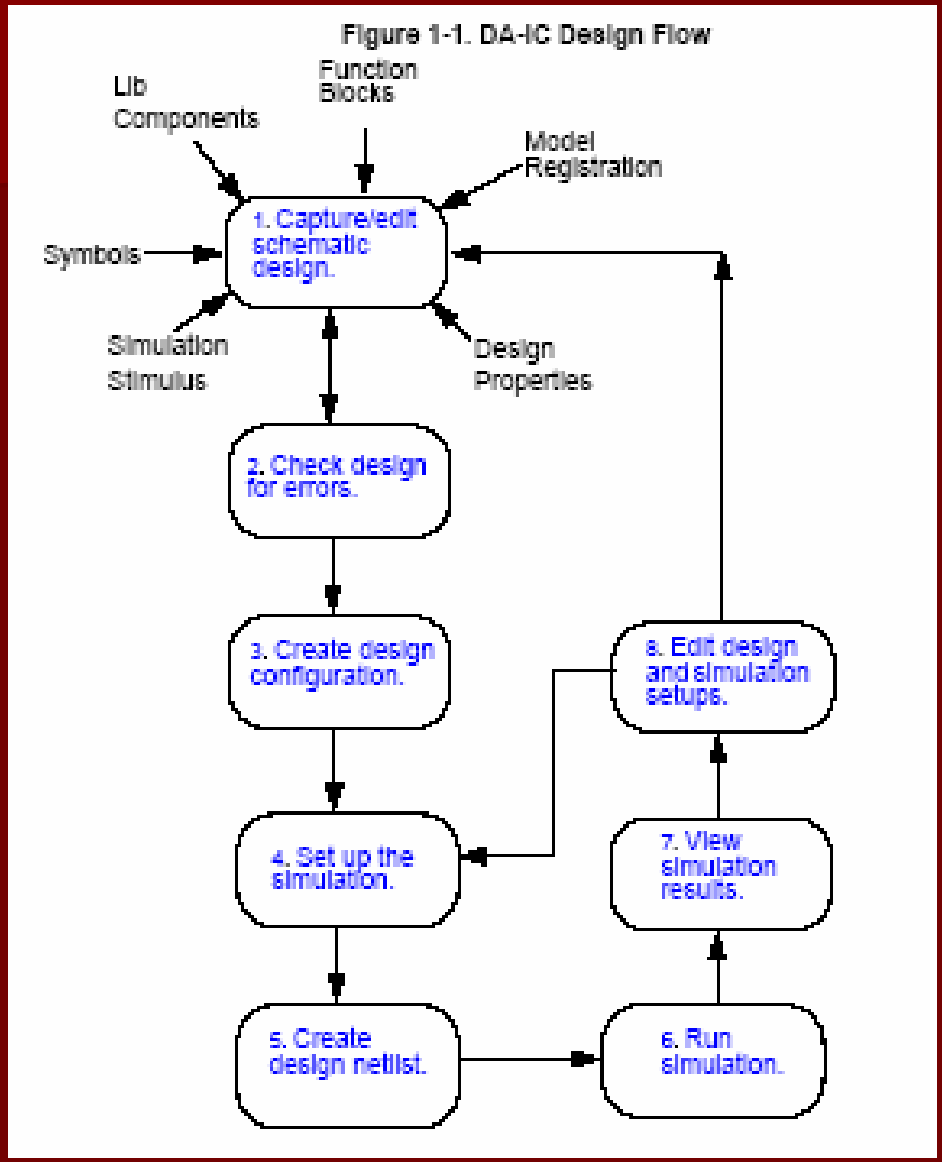
Xilinx “ISE”
Altera “Max Plus 2”



Physical Design – ASIC (Std. Cell)



Design Architect-IC Design Flow



Preparation for Layout

- Convert Verilog netlist to Mentor Graphics "EDDM" netlist format
  - Invoke Design Architect-IC *(adk_daic)*
  - "Import Verilog" feature to create schematic
    - mapping file $ADK/technology/adk_map.vmp
  - Open the generated schematic
  - Prepare "design viewpoints" for layout
- May also create schematic diagrams for "hand-designed" circuits – gate and/or transistor level
  - Components from ADK library